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INVESTIGATIONS ON THREE PHASE FIVE SWITCH MULTILEVEL INVERTER WITH REDUCED NUMBER OF SWITCHES

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ABSTRACT

The multi-level inverter system is mostly used in ac drives, when both reduced harmonic contents and high power are required. In this paper a new topology of multilevel inverter is introduced. This type has many steps with less power electronic switches. Due to the less number of switches the cost of the inverter is very less and also less installation area is required. Firstly, we describe briefly the structural parts of the inverter then switching strategy and operational principles of the proposed inverter are explained and operational topologies are given. Simulation is performed using MATLAB SIMULINK. Various conventional PWM techniques are applied to the circuit such as PDPWM, PODPWM, APODPWM, VFPWM and COPWM. By comparing among the conventional PWM techniques, PDPWM provide the less THD value and COPWM provide a higher fundamental RMS output voltage.

Keywords: THD, PD, POD, APOD, VF, CO.

Contribution/ Originality

This study contributes various PWM techniques and hence this work presents a novel approach for controlling the harmonics of output voltage of chosen MLI employing Sinusoidal references for different PWM switching strategies.

1. INTRODUCTION

Multilevel power converter is a generic term applied to power converters with topologies capable of synthesizing multi-tier voltage waveforms and processing high voltage by means of series connection of active devices to many discrete DC voltage sources. Ingenious interconnection of power devices to split DC rail increase the voltage handling capability of these converters for given power devices. The multilevel inverter [MLI] is used for high voltage and high power applications. This inverter produce staircase (stepped) waveform from several different levels of DC voltage. The MLI provide lower voltage rating of devices, low harmonics

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distortion, high power quality waveforms, lower switching frequency and losses, higher efficiency, reduction of dv/dt stresses. Because of the above characteristics, it have a possibility of working with low speed semiconductors if its comparison with the two-level inverters. Many number of MLI topology are available but most popular MLI topology is Diode Clamped, Flying Capacitor and Cascaded Multilevel Inverter. Radan, et al. [1] introduced an evaluation of carrier based PWM methods for multi level inverters. José, et al. [2] proposed multilevel voltage source converter topologies for industrial medium voltage drives. McGrath and Holmes [3] introduced a general analytical method for calculating inverter dc link current harmonics. Palanivel and Dash [4] proposed multicarrier pulse width modulation methods based three phase cascaded multilevel inverter including over modulation and low modulation indices. Pan and Peng [5] introduced a sinusoidal PWM method with voltage balancing capability for diode clamped five level converters. Konstantinou and Agelidis [6] deal with a performance evaluation of half bridge cascaded multilevel converters operated with multicarrier sinusoidal PWM techniques. Al-Judi, et al. [7] deal with a modified cascaded multilevel inverter with reduced switch count employing bypass diodes. Rokan, et al. [8] made a new multilevel inverter topology with reduced number of switches. Suroso and Toshihiko [9] discussed a multilevel voltage-source inverter using h-bridge and two level power modules with a single power source. Bayat and Babaei [10]a new cascaded multilevel inverter with reduced number of switches. Ho-Dong, et al. [11]multi-level inverter capable of power factor control with dc link switches.

2. MULTILEVEL INVERTER

In this work a new topology of multilevel inverter is introduced. The basic operation can be described as sequential stacking of a number of DC voltage source stages which depends on certain time of operation that one stage is stacked (forward or reverse) or bypassed.

The order of numbering of the switches for R - phase is Sa_1, Sa_2, Sa_3, Sa_4, Sa_5, Sa_6 and Sa_7. This circuit does not have a capacitor and diode. The voltage levels of the outputs are $4V_{dc}$, $3V_{dc}$, $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$, $-4V_{dc}$. Fig.1 shows a three phase five switch per phase seven level inverter. The operation of a multilevel inverter is concerned with comparison of carrier and reference wave. MLIs also have some issues such as necessitate a big number of semiconductor switches which increases as the number of steps/levels increases. If the levels of the steps increase the design will be multifarious for synchronous gate drivers for different levels. The order of numbering of the switches is Sa_1, Sa_2, Sa_3, Sa_4 and Sa_5. This circuit does not have a capacitor and diode. So price tag of the circuit is low compared to the conventional circuit. Fig.1 (a) shows the construction of signal from the block diagram.

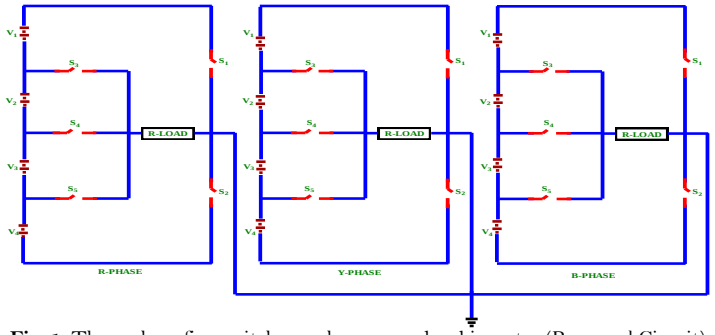

Fig-1. Three phase five switch per phase seven level inverter (Proposed Circuit)

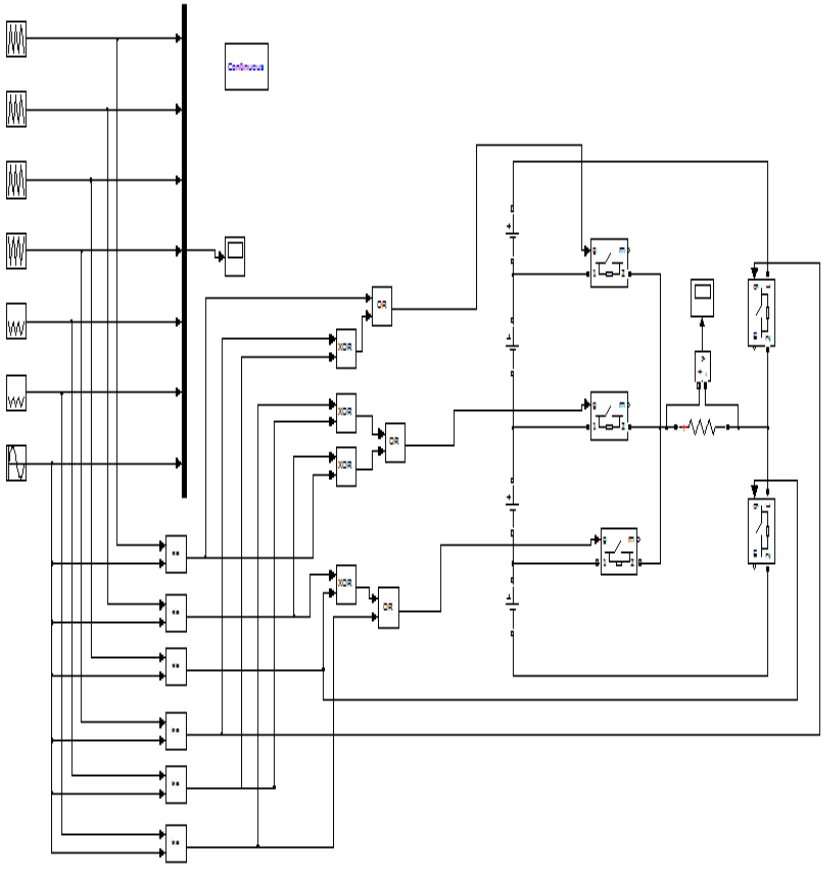

Fig-1. (a) Construction of signal from the block diagram (Proposed Circuit, Per phase)

The voltage level of the outputs are $3V_{dc}$, $2V_{dc}$, V_{dc}, 0, - V_{dc}, $-2V_{dc}$, $-3V_{dc}$. In proposed circuit semiconductor switches are less when compared to the conventional circuit. So the advantages of the proposed circuit are fewer cost and minimum switching losses. Fig.1. shows a three phase seven level inverter. Fig. 1(b), 1(c) and 1(d) shows the conventional three phase Diode Clamped Multilevel Inverter (DCMLI), three phase Flying Capacitor Multilevel Inverter (FCMLI) and three phase Cascaded Multilevel Inverter (CMLI). Table 1 displays the comparison between conventional and proposed circuit.

Table-1. Comparison between conventional and proposed circuit

S.NO	Conventional circuit DCMLI (7-level)	Conventional circuit FCMLI (7-level)	Conventional circuit CMLI (7-level)	Proposed circuit (7-level)
Number of switches	36	36	36	**15**
Number of main diode	36	36	36	**0**
Number of clamping diode	36	0	0	**0**
Number of DC bus capacitor	18	18	18	**0**
Number of balancing capacitor	0	45	0	**0**

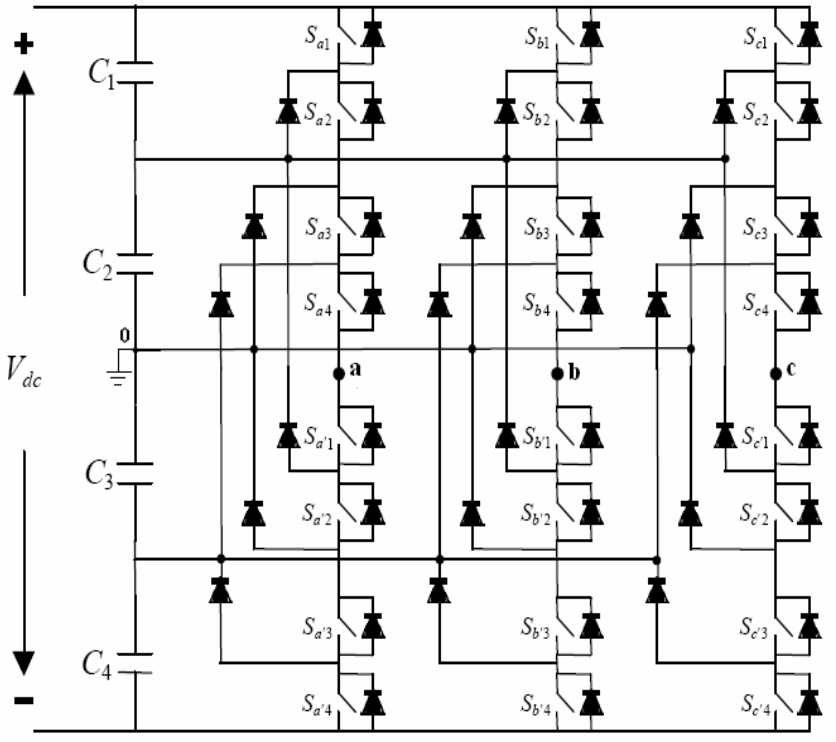

Fig.-1. (b) A Three Phase Diode Clamped Five level Inverter (Conventional DCMLI)

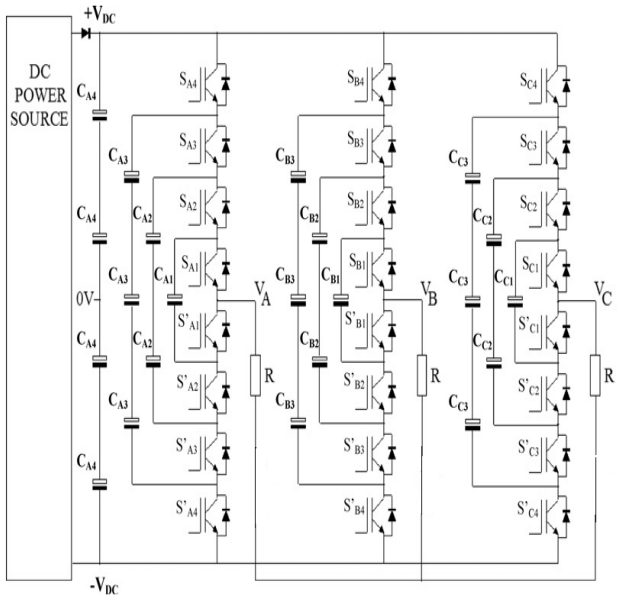

Fig-1. (c) A Three Phase Flying Capacitor Five level Inverter (Conventional FCMLI)

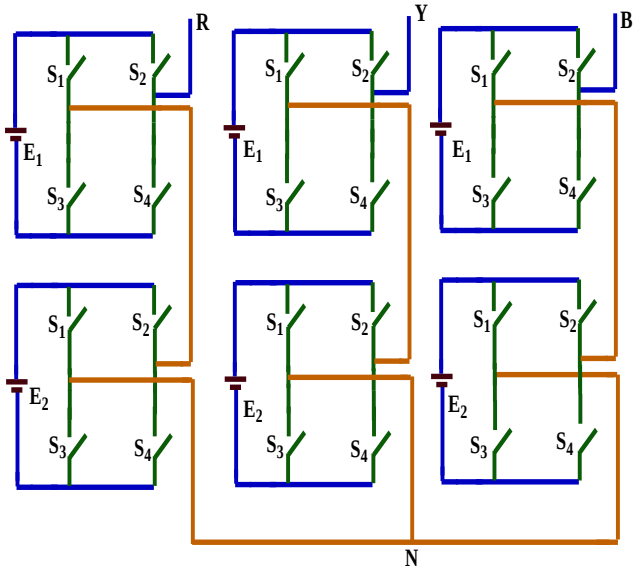

Fig-1. (d) A Three Phase Five level Cascaded Multilevel Inverter. (Conventional CMLI)

3. MODULATION STRATEGY

The most standard PWM methods are available to the inverter. For controlling the output voltage, one of the method is SPWM method. In this method, a fixed DC input voltage is applied to the inverter and get a controlled AC output voltage by adjusting the ON and OFF periods of the inverter power semiconductor devices. By this technique increasing the switching frequency of the PWM pattern reduces the lower frequency harmonics by moving the switching frequency

carrier harmonics and associated sideband harmonics further away from the fundamental frequency component. The modulating/reference wave of multilevel carrier based PWM strategies is sinusoidal. The sinusoidal reference wave is concerned to multiple Control Freedom Degree including frequency, amplitude, and phase angle of the reference wave. The principle of SPWM strategy is to employ the several carriers with three phase sinusoidal modulating signal. For an m level inverter, m-1 carriers are used. All carriers having same frequency f_c and same peak-to-peak amplitude A_c which are disposed such that the bands they occupy overlap each other. Fig. 2 shows a sample SIMULINK model developed for chosen multilevel inverter. The amplitude of the reference wave is A_m and frequency is f_m, which are centered in the middle of the carrier signals. The frequency ratio m_f is defined in the carrier overlapping method as follows:

$$m_f = \frac{f_c}{f_m} \qquad (1)$$

This paper focuses on five SPWM strategies. They are: PDPWM, PODPWM, APODPWM, VFPWM and COPWM.

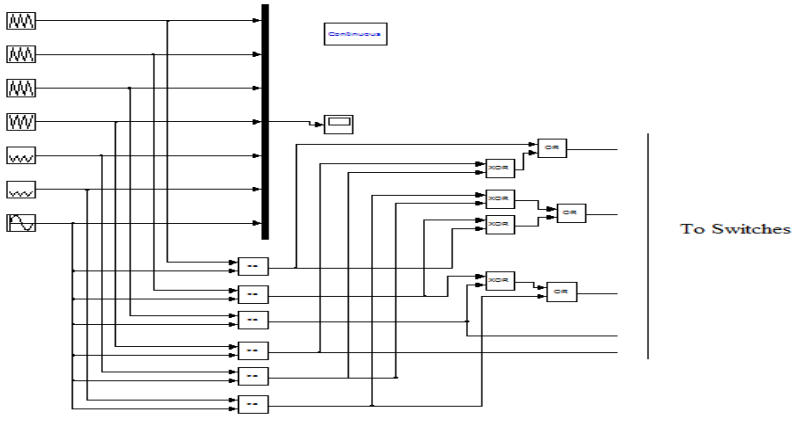

Fig-2.A sample SIMULINK model developed for chosen multilevel inverter (Per phase)

Table-2. Switching Table for asymmetrical multi level inverter

SwitchingLevel	S_1	S_2	S_3	S_4	S_5
3 V_{dc}	0	1	0	0	1
2 V_{dc}	0	1	0	1	0
V_{dc}	0	1	1	0	0
0	0	0	0	0	0
-V_{dc}	1	0	0	0	1
-2 V_{dc}	1	0	0	1	0
-3 V_{dc}	1	0	1	0	0

3.1. PDPWM Strategy

This method is one of the PWM techniques. In this work, six carriers are applying for chosen MLI. All carriers are having amplitude as one volt. The sinusoidal reference wave is placed at the middle of the six carriers. In PDPWM technique all carriers are established in a same manner. In the present work, the multi-carrier based phase disposition PWM scheme is used. In sine-triangle method for a seven-level inverter where in modulation or sinusoidal reference signal is compared with six (m-1 in general) triangle waveform when the number of output voltage level is 7 (= m), 6 (m −1) carrier waveforms are arranged so that every carrier is in phase. Fig.3 shows the modulating and carrier waveform for PDPWM strategy.

The carriers are in phase across all the bands. For this technique, significant harmonic energy is concentrated at the carrier frequency but since it is a co-phasal component, it doesn't appear in the line-to-line voltage.

$$\text{The frequency modulation index } m_f = \frac{f_c}{f_m} \tag{2}$$

$$\text{The amplitude modulation index } m_a = \frac{2A_m}{A_c(m-1)} \tag{3}$$

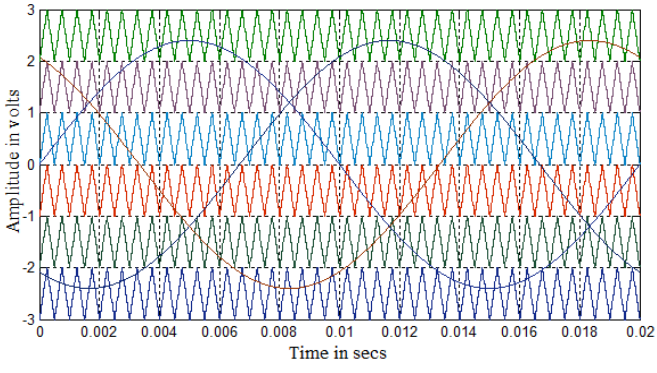

Fig-3. Modulating and carrier waveforms for PDPWM strategy (m_a=0.8 and m_f=40)

3.2. PODPWM Strategy

This method is same as PDPWM but carrier establishment is different. The carriers are uniformly divided into two groups based on positive/negative average levels. In this type the two groups are opposite in phase with each other while remaining in phase surrounded by the group. Fig.4 shows the modulating and carrier waveform for PODPWM strategy.

For POD modulation all carrier waveforms above zero reference are in phase and they are 180^0 out of phase with those below zero. When the number of level is m (= 7) , m − 1 (= 6) carrier waveforms are arranged so that all carrier waveforms above zero are in phase and are 180^0 out of phase with those below zero. The significant harmonics are located around the carrier frequency for both the phase and line-to-line voltage. Formula for m_a and m_f are same as that of PDPWM technique.

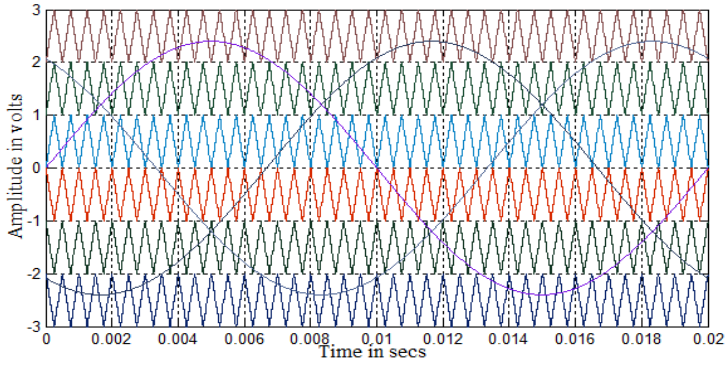

Fig-4. Modulating and carrier waveforms for PODPWM strategy (m_a=0.8 and m_f=40)

3.3. APODPWM Strategy

This method is also same as PDPWM technique but one of the main different in APODPWM by evaluate to the PDPWM is that the alternate carriers are phase altered by 180 degree with each other. Fig.5 shows the modulating and carrier waveform for APODPWM strategy. In case of APOD modulation, every carrier wave is out of phase with its neighbour carrier by 180 degree. Since APOD and POD schemes in case of three level inverter are the same, a seven level inverter is considered to discuss about the APOD scheme. When the number of level m (= 7) , m − 1 = 6 carrier waveforms are arranged so that every carrier waveform is in out of phase with its neighbor carrier by 180^0. Carriers in adjacent bands are phase displaced by 180°. With this method, the most significant harmonics are centered as side bands around the carrier. Formula for m_a and m_f are same as that of PDPWM strategy.

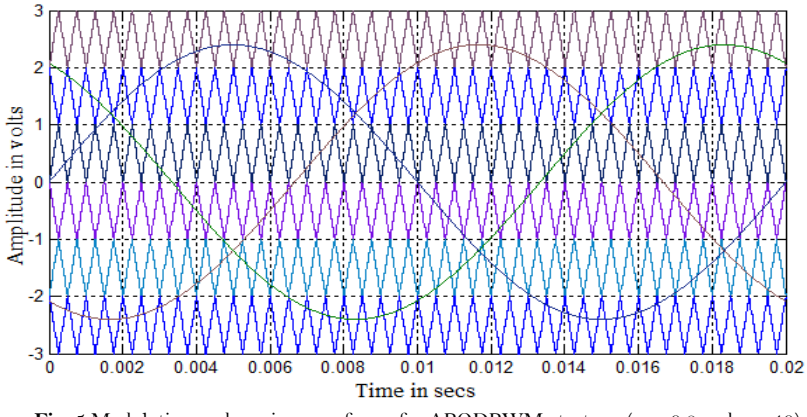

Fig-5. Modulating and carrier waveforms for APODPWM strategy (m_a=0.8 and m_f=40)

3.4. VFPWM Strategy

This method is one of the PWM techniques and it is same as PDPWM but intermittent carrier having different frequency compare to upper and lower carrier. Fig.6 shows the modulating and carrier waveform for VFPWM strategy. The number of switching for upper and lower devices of chosen DCMLI is much more than that of intermediate switches in above PWM strategies using constant frequency carriers. In order to equalize the number of switching's for all

the switches, VFPWM strategy is used in which the carrier frequency of the intermediate switches is properly increased to balance the numbers of switching for all the switches. The amplitude modulation index for VFPWM strategy is

$$m_a = \frac{2A_m}{(m-1)A_c} \quad (4)$$

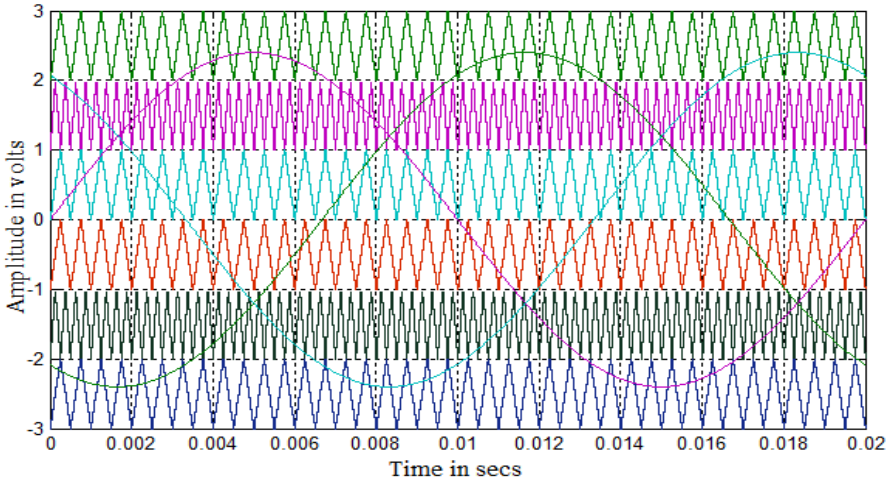

Fig-6. Modulating and carrier waveforms for VFPWM strategy ($m_a = 0.8$, $m_f = 40$ for upper and lower switches and $m_a = 0.8$,$m_f = 80$ for intermediate carrier)

3.5. COPWM Strategy

This method is same as PDPWM method but all carriers are overlapped each other and overlapping amplitude is 0.8V but each carrier having amplitude 1.6V and the total amplitude of this technique is 2.8. The carrier arrangement for this strategy is shown in Fig.7. The COPWM-A method utilizes the CFD of vertical offsets among carriers. The principle of COPWM-A is to use several overlapping carriers with single modulating signal. For an m level inverter, m-1 carriers with the same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy overlap each other. The overlapping vertical distance between each carrier is $A_c/2$ in this work. The reference wave has the amplitude A_m and frequency f_m and it is centered in the middle of the carrier signal. Within this COPWM strategy, combination of varied vertical and/or horizontal offsets are adopted to get different species such as COPWM-A, COPWM-B and COPWM-C. The amplitude modulation index is

$$m_a = \frac{A_m}{\left(\frac{m}{4}\right) * A_C} \quad (5)$$

Actually COPWM-A and COPWM-C can be looked on as a second control freedom degree change besides offset in vertical: the carriers have horizontal phase shift from COPWM-A.

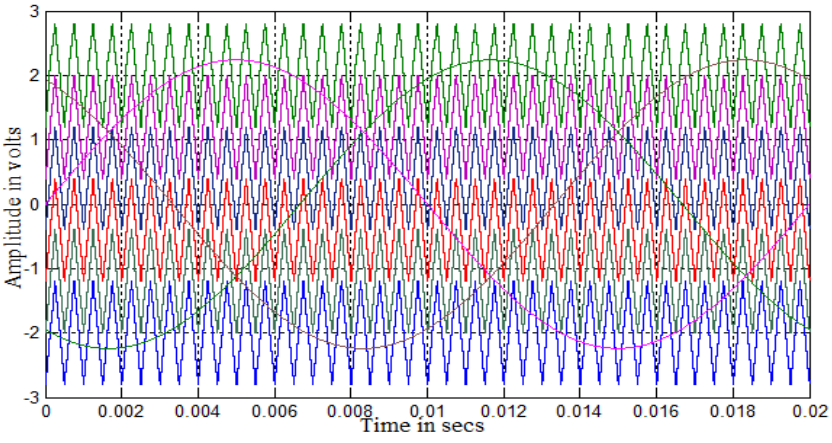

Fig-7. Modulating and carrier waveforms for COPWM strategy (m_a=0.8 and m_f=40)

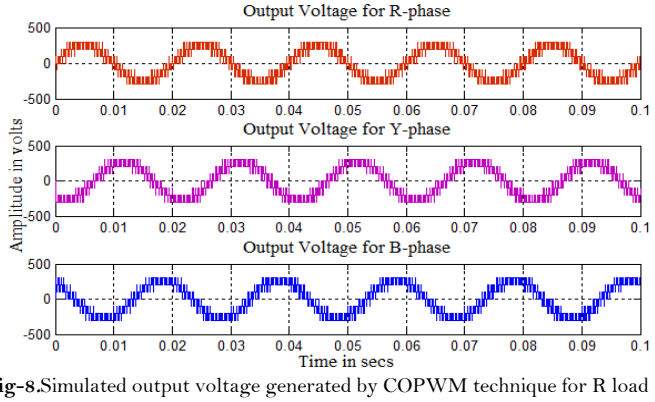

Fig-8. Simulated output voltage generated by COPWM technique for R load

Actually COPWM-A and COPWM-C can be looked on as a second control freedom degree change besides offset in vertical: the carriers have horizontal phase shift from COPWM-A.

4. SIMULATION RESULT

The three phase chosen seven level inverter is modelled in SIMULINK using power system block set. Switching signals for MLI are developed using sinusoidal PWM techniques discussed previously. Simulation is performed for different values of m_a ranging from 0.97 – 1. The corresponding %THD values are measured using FFT block and they are shown in Tables 3. Next table displays the V_{RMS} of fundamental of inverter output for same modulation indices.

The followings are observed from the FFT spectra:

(a) Harmonic energy above 3 % is present in (i) 2^{nd}, 6^{th}, 8^{th}, 10^{th}, 12^{th}, 18^{th}, 20^{th}, 24^{th}, 26^{th}, 32^{nd}, 36^{th} and 38^{th} orders in PDPWM strategy. (ii) 34^{th}, 35^{th}, 37^{th}, 38^{th}, 39^{th} and 40^{th} orders in PODPWM strategy. (iii) 29^{th}, 33^{rd}, 35^{th} and 39^{th} orders in APODPWM strategy. (iv) 6^{th}, 10^{th}, 12^{th}, 18^{th}, 24^{th}, 26^{th}, 28^{th}, 30^{th}, 32^{nd}, 36^{th} and 38^{th} orders in VFPWM strategy. (v) 5^{th}, 7^{th}, 11^{th}, 18^{th}, 20^{th}, 26^{th}, 36^{th}, 38^{th} and 39^{th} orders in COPWM strategy.

(b) 2^{nd} harmonic are dominant in PDPWM strategy.

(c) Dominant lower side band harmonic (40^{th} order) is not present in all PWM strategies.

(d) PDPWM and VFPWM contain more number of dominant harmonics.

(e) Among the five strategies APODPWM and PODPWM contain minimum harmonic energy whereas least number of harmonics exists in APODPWM strategy.

(f) Among the various PWM strategies, APODPWM contain relatively minimum harmonic energy with the least number of dominant harmonics.

The following parameter values are used for simulation: V_{dc}=110V, f_c=2000Hz, f_m=50Hz and R (load) = 100 ohms

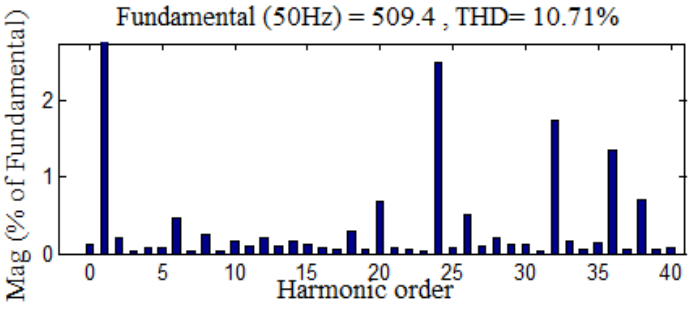

Fig-9.FFT spectrum for PDPWM technique

Table-3.% THD of Output Voltage of Chosen MLI for Various Values Of Modulating Indices

m_a	PD	POD	APOD	VF	CO
1	10.86	15.30	14.99	13.36	13.68
0.99	10.73	15.80	15.39	13.50	13.64
0.98	10.71	16.57	15.73	13.52	13.59
0.97	10.97	17.36	16.21	13.77	13.47

Table-4.V_{rms} (Fundamental) Of Output Voltage Of Chosen MLI For Various Values Of Modulating Indices

m_a	PD	POD	APOD	VF	CO
1	367.3	366.8	367.1	367.3	388.9
0.99	363.7	363.9	362.8	363.7	386.9
0.98	360.2	359.9	359.9	360.2	384.2
0.97	355.9	356.0	356.1	356.1	380.9

Table-5. Form Factor of Output Voltage of Chosen MLI for Various Values of Modulating Indices

m_a	PD	POD	APOD	VF	CO
1	2295.6	12226.6	12236.6	6121.6	3889
0.99	2273.1	12130.0	12126.6	7274.0	3224.1
0.98	2770.7	11996.6	11996.6	36020	1600.8
0.97	2542.1	11866.6	11870.0	17805	2240.5

Table-6. Crest Factor of Output Voltage of Chosen MLI for Various Values of Modulating Indices

m_a	PD	POD	APOD	VF	CO
1	1.4143	1.4141	1.4140	1.4143	1.4139
0.99	1.4143	1.4141	1.4142	1.4140	1.4140
0.98	1.4142	1.4140	1.4142	1.4139	1.4143
0.97	1.4144	1.4143	1.4149	1.4139	1.4140

Table-7. Distortion Factor of Output Voltage of Chosen MLI for Various Values of Modulating Indices

m_a	PD	POD	APOD	VF	CO
1	0.0183	0.0463	0.0574	0.0249	0.0178
0.99	0.0203	0.0624	0.0512	0.0360	0.0175
0.98	0.0195	0.0700	0.0524	0.0262	0.0180
0.97	0.0201	0.0595	0.0358	0.0277	0.0258

5. CONCLUSION

In this paper various new proposal adopting the constant switching frequency multicarrier CFD concepts are developed and simulated for chosen seven level inverter. Performance indices like %THD, V_{RMS} (indicating the amount of DC bus utilization), CF, FF and DF related to power quality issues have been evaluated, presented and analyzed.By comparing among the conventional PWM techniques, PDPWM technique offers the less THD value (table 3) and COPWM offer a higher fundamental RMS output voltage (table 4).Table 5 shows FF for all modulating indices. Table 6 displays CF for all chosen modulating indices. Table 7 displays DF for all chosen modulating indices. The result indicate that appropriate strategies have to be employed depending on the performance measure required in a particular application of MLI based on the criteria of output voltage quality (Peak value of the fundamental, THD and dominant harmonic components).

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