Review of Computer Engineering Research
2026 Vol. 13, No. 3, pp. 86-100
ISSN(e): 2410-9142
ISSN(p): 2412-4281
DOI: 10.18488/76.v13i3.5103

A transmission-gate-based low-power CMOS half-adder with an antileak sleep-transistor method for industrial sustainability

Mohammed Altaf Ahmed[1+]
Suleman Alnatheer[2]
Qutubuddin Mohammed[3]

[1,2]*Department of Computer Engineering, College of Computer Engineering and Sciences, Prince Sattam bin Abdulaziz University, Al-Kharj, Saudi Arabia.*
[1]*Email: m.altaf@psau.edu.sa*
[2]*Email: s.alnatheer@psau.edu.sa*
[3]*Department of Electrical Engineering, College of Engineering Wadi Addawasir, Prince Sattam Bin Abdulaziz University, Saudi Arabia.*
[3]*Email: q.mohammed@psau.edu.sa*

(+ Corresponding author)

Article History
Received: 3 November 2025
Revised: 6 February 2026
Accepted: 16 March 2026
Published: 19 August 2026

Keywords
Antileak with sleep transistor
CMOS processing
Industrial sustainability
Leakage power reduction
Low-power VLSI.

ABSTRACT

The digital integrated circuits (ICs) are becoming increasingly complex as technology advances daily. Conventional digital ICs often suffer from high transistor counts, large chip areas, and increased power consumption during implementation. Maintaining these parameters at appropriate levels is essential to ensure the efficiency and sustainability of semiconductor technologies. This research proposes a technique using a CMOS transistor and a transmission gate to develop an optimized integrated circuit (IC). It presents a transmission gate approach to replace the existing CMOS implementation in commercially available ICs. Additionally, it introduces a method for reducing leakage power through an improved physical design of a laydown sleep transistor that utilizes the Antileak method. A digital logic circuit of a half-adder cell is implemented using both the conventional CMOS method and the proposed hybrid technique. Comparing the results from both methods, it is evident that the proposed approach is significantly better in terms of cost, power, and area performance. The Antileak laydown sleep transistor reduces leakage power and helps lower overall power consumption. Therefore, the proposed technique for digital ICs offers low-cost, energy-efficient, and area-optimized solutions, supporting sustainability in the semiconductor industry and serving as a viable alternative for future IC development.

Contribution/Originality: This study offers a novel contribution to the semiconductor industry by maintaining the yield of the product. The study employs a novel technique to minimize chip area and power consumption while comparing it with other conventional methods. The paper's primary contribution is to establish a reasonable matrix that reduces power consumption and area and improves yield.

1. INTRODUCTION

The complementary Metal-Oxide-Semiconductor (CMOS) technique is always a dominant method for developing Very Large-Scale Integration (VLSI). The CMOS transistor has always existed in ICs as an integral part for several decades. Since the invention of integrated circuits (ICs), reducing the number of transistors has been necessary and has consistently posed a significant challenge for researchers. As technology improves, the transistor count in ICs increases from thousands to millions [1]. Handling such a dense transistor IC becomes complicated when trying to achieve low cost and high performance [2]. Therefore, it becomes essential to maintain a reasonable characteristic between transistor count and performance in power, speed, and cost. To achieve this, current research aims to enhance the existing method at the physical design level by reducing the transistor count in the IC and

improving performance. The CMOS transmission gate replaces the CMOS transistor implementation method for developing the VLSI chip. The memory and other logic components of very-large-scale integration (VLSI) systems occupy a large area and consume more power. Therefore, designing hardened components for various blocks with low cost and high performance has gained much importance [3]. Conventionally, the hardening methods of time redundancy and modular redundancy are commonly used for easy design to attain considerable hardware, power, and performance concerns. The research [4] uses a C-element filter hardening method for sequential circuits. This method of filtering requires a single-event transient pulse, but determining pulse width is challenging. Furthermore, feedback control systems cause increased power and complexity in the design [5]. This unwanted pulse is masked by the method of the Schmitt trigger (ST) buffer with hysteresis characteristics [6, 7]. Complementary metal-oxide-semiconductor (CMOS)-based devices, with a minimum feature size of 20 nm to 40 nm, dominate advanced VLSI chip fabrication. The scaling of very-large-scale integration (VLSI) technology increases transistor counts in ICs and chip density. The high density of integrated circuits (ICs) results in extensive interconnections, which enhance capacitive coupling among them, creating new opportunities and challenges for engineers to address.

Therefore, to tackle these discussed issues, this research proposes a CMOS implementation using a transmission gate to reduce transistor count and a hardened components approach for a low-cost, high-performance VLSI design approach for IC fabrication. The methods in the research [8-11] are presented by CMOS transistor implementation. Whereas power consumption, delay, and crosstalk have been tackled in the research [12-16]. The research [17-23] investigates power reduction methods using LECTOR and other techniques. These conventional methods use large transistors with external sleep signals. The leakage is cut only during explicit sleep mode, and their delay and overhead area are greater compared to the proposed small transistor pair with very negligible switch time. We have further reduced the transistors and improved performance at an acceptable level compared with existing methods. The processing of the circuit estimates the physical level design and layout at different layers, and the effects of crosstalk, delay, and noise with leakage current have also been reduced.

The half-adder cell in this research study is implemented with only eight transistors. As the transmission gate is a known approach, the implementation of the 8T half-adder cell demonstrates a notable level of design efficiency. Other methods use more transistors to implement the same circuit. Modern chip designs integrate millions to billions of transistors on a single chip; therefore, reducing the number of transistors by even a few can significantly impact overall performance and results. Consequently, in this research, we strive to maintain the transistor size as reasonably as possible to achieve the desired functioning. We carefully construct the transistors according to design rules during the fabrication process. Furthermore, we extend the research by proposing the Antileak technique, which uses a lay-down sleep transistor to limit leakage power. The main objective of the research is to reduce power consumption in digital circuits by decreasing the number of hardware components. Additionally, the research aims to develop a technique that reduces leakage power using an antifuse method, which will contribute to maintaining a sustainable industrial environment.

The rest of the paper is structured as follows: Section 2 covers the methodology. Section 3 presents experimental results and comparisons with existing methods. Section 4 discusses the discussion, and Section 5 outlines the conclusion and future scope.

2. LITERATURE REVIEW

The advancements in IC technology are characterized by features such as low area, reduced power, and high-performance efficiency. It always becomes a challenge for the semiconductor industry to maintain these characteristics. Low-power digital circuit design has emerged as a pivotal field of study as CMOS technology advances into deep-submicron domains, where leakage power and reliability challenges increasingly affect system performance. A commonly used digital logic as a more fundamental building block is an adder cell, which is used in recent high-

end processors and other logic designs. Consequently, numerous studies have focused on optimizing the transistor-level implementations of adder cells for power efficiency, area reduction, and fault tolerance.

Azimi, et al. [24] examined a radiation-hardened CMOS full adder by implementing selective transistor duplication at the layout level to enhance resilience against soft-error occurrences, illustrating the significance of transistor-level modifications in improving circuit reliability at advanced technology nodes, albeit with some area overhead and delay penalty [24].

Similarly, El-Maleh, et al. [25] studied defect-tolerant structures and developed a compact N^2-transistor configuration aimed at making nanoscale digital design more fault-tolerant. The work demonstrates that transistor-efficient architectures remain a primary goal as process variations and leakage currents increase with technology scaling [25]. The research continued to build on architectural improvements and also explored ways to reduce power consumption in arithmetic circuits, such as adders; for instance, John [26] designed a power-efficient Kogge–Stone adder by use of an OR gate optimized for the 45 nm CMOS process, which highlights the importance of gate-level and device-level refinements in decreasing overall dynamic and static power consumption in high-performance adder circuits [26].

Even though the transistor count is reduced by some research, the leakage static power remains a major challenge, especially while dealing with a nanoscale chip design. The problem was therefore addressed in several studies by combining pass-transistor and TG logic approaches with some other power-lowering methods, such as gating and threshold-voltage selection. For instance, a work from 2024 talks about a complete adder that uses a modified swing-restored complementary pass-transistor logic to cut down on power loss while retaining performance [27]. Another study of low-voltage full adder designs shows that trade-offs in design often mean finding a balance between the number of transistors, driving output ability, and the power reduction procedures (Short circuit, limit leakage, etc.) [28].

There is also a growing interest in combining logic-style efficiency with ways to stop leakage, like power-gating or leakage-control transistors. In this context, this research study suggests a half adder design implementation with only 8 transistors that employs transmission-gate logic and the LECTOR anti-leak approach to stop leaks without external sleep signals.

The presented method differs from regular power-gating techniques that use large pull-up and pull-down transistors at the block level to achieve the desired goal. Instead, it uses a LECTOR method that employs a small leakage-control transistor inside the logic network itself to prevent leaks in the circuit. This way, at least one transistor in the leakage path remains close to cut-off for any input combination, which dynamically lowers static leakage and provides significant power reduction while enabling large-scale applications.

This design method fits with the trend of combining hybrid logic with ways to prevent leakage as IC complexity increases. Previous studies have shown that hybrid-logic full adders are useful. For instance, Kandpal, et al. [10] 10-T XOR–XNOR–based hybrid logic full adder works quickly and uses transistors efficiently [29]. These designs demonstrate that compact, pass-transistor/TG-based adders can function effectively; however, they often neglect to address methods for minimizing leakage through internal control transistors such as LECTOR.

The proposed study presents an innovative contribution by incorporating LECTOR into a minimal TG-based half adder, achieving a unique synergy of logic-level efficiency (8T TG design) and transistor-level leakage control. This results in a substantial reduction in static power without compromising output swing or significantly increasing the transistor count. Based on the studies mentioned above and our research, it is clear that combining compact logic styles (like TG and hybrid logic) with leakage-control methods (like LECTOR) is a promising way to design arithmetic circuits for VLSI systems that use a lot of power and have high density. This approach is especially relevant for contemporary CMOS process nodes, where leakage is a significant problem.

3. METHODS

CMOS (Complementary Metal-Oxide-Semiconductor) technology is the most significant aspect of current chip design because it uses very little power, is particularly resistant to noise, and can be scaled up or down to fit millions to billions of transistors on a single chip. Digital logic circuits, memory devices, and microprocessors heavily utilize it. The key advantages of CMOS are that it requires less static power and can cram many circuits into a small space. This enables the creation of smaller and more power-efficient electronic systems. As device sizes shrink and human behavior becomes more dependent on these devices, new challenges arise that force CMOS technology to operate smoothly under increased load and hardware demands. As technology advances, maintaining the short channel length and managing leakage current limitations become increasingly challenging. In this research, we aim to reduce the hardware in the CMOS circuit to minimize its size and power consumption. The methodology also aims to reduce leakage power. The half-added cell is considered for experimental purposes.

In this research, we have implemented a half-adder cell using a compact 8-transistor CMOS model that combines transmission-gate logic with the LECTOR anti-leakage technique. The transmission-gate structure minimizes the transistor count without affecting the logic level swing, and the LECTOR method is responsible for the self-leakage-control transistors within the pull-up and pull-down paths to suppress subthreshold leakage without external sleep signals. whereas the previous studies primarily focus on reducing transistor count or improving speed using hybrid or pass-transistor logic. The proposed model simultaneously addresses logic-level efficiency and continuous leakage reduction to improve the performance, efficiency, and cost reduction in digital ICs. Implementation and validation using the Microwind tool further demonstrate lower power dissipation compared to conventional CMOS and previously reported half-adder designs, as demonstrated in the results section.

3.1. Half-Adder Cell in CMOS

The half-adder cell is implemented on CMOS 0.12 µm technology. It is implemented in CMOS logic by using a proposed CMOS transistor with a transmission gate approach. The block diagram of the half-adder is shown below. The circuit has two inputs, A and B, and two outputs, sum and carry, with a single XOR gate and a single AND gate, as shown in Figure 1. We compare the transistor count, power consumption, and various delays of the half adder cell using these two methods.

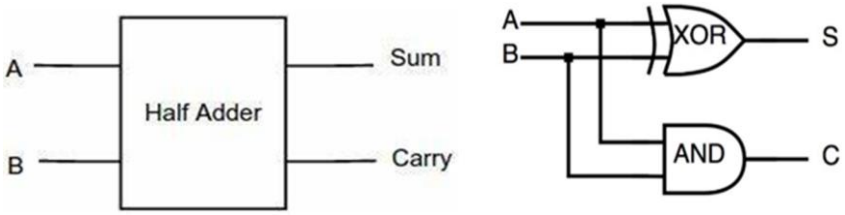

Figure 1. Half-Adder Cell.

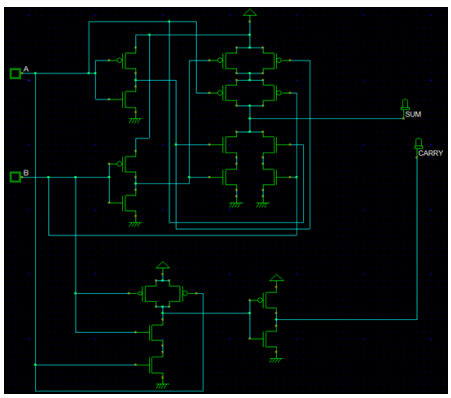

Figure 2. Half Adder CMOS (DSCH3.8).

Figure 2 Half-Adder CMOS the conventional method of CMOS implementation of the Half-Adder Cell consists of one XOR gate and one AND gate. The XOR gate is implemented using two inverters and AND-OR logic, and it uses a total of 12 transistors. The AND gate is implemented using NAND and an inverter, and it uses six transistors. Therefore, this half-adder cell uses a total of 18 transistors. The schematic diagram is shown in Figure 2, which uses the DSCH3.8 tool.

CMOS Implementation of a Half-adder cell.

Pull-up network.

Sum= AB'+A'B.

Carry = AB= NOT (AB)'.

Pull-down network.

Sum'=A'B'+AB.

Carry'= A'+ B'.

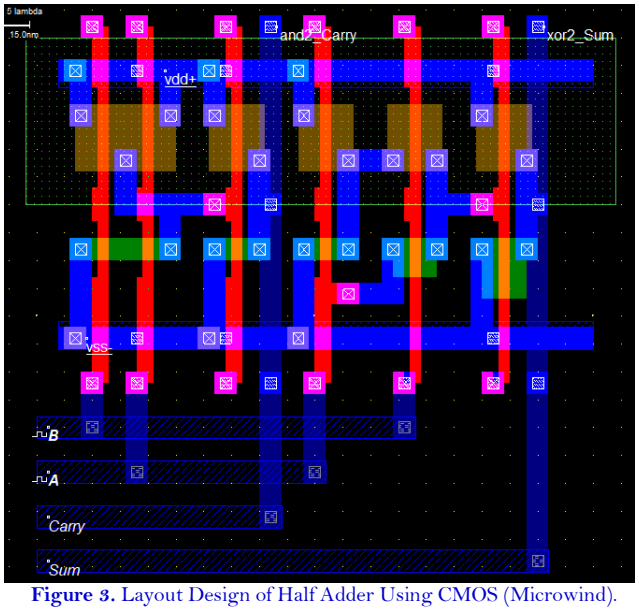

Figure 3. Layout Design of Half Adder Using CMOS (Microwind).

Simulations of the circuit are carried out and are placed in the Results section. The layout is designed for the half-adder cell on Microwind 3.8 tool and is shown in Figure 3. It is designed on 0.12µm technology; the power consumption and the delays are also calculated.

3.2. Development of the Half-Adder Cell using the Proposed Technique

In this method, we proposed a half-adder cell using CMOS transistors and the transmission gate. We implement an XOR gate and one AND gate in this research with only eight transistors. Figure 4 shows the circuits, which use one transmission gate, two inverters, and two additional transistors. One XOR gate and one AND gate are implemented using only eight (8) transistors. Using the proposed implementation method, we reduced ten transistors if we compare with the conventional method of CMOS implementation and six transistors with the implementation of the transmission gate and an AND gate. The layout is also developed on the Microwind tool and is shown in Figure 5. The functional waveforms are developed in the results section. The proposed method of developing logic design will have more impact when we address digital systems where millions of transistors are used to implement the circuit or the system. As a result of this approach, the chip area will significantly reduce, which will help minimize power consumption and delay in the overall system.

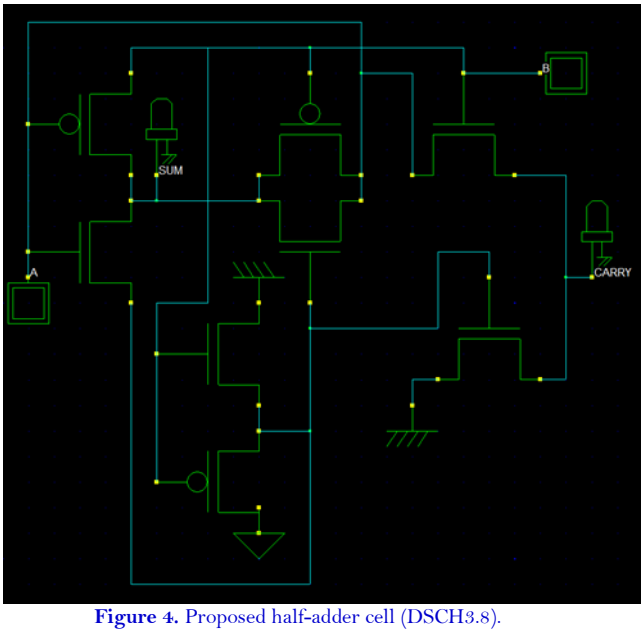

Figure 4. Proposed half-adder cell (DSCH3.8).

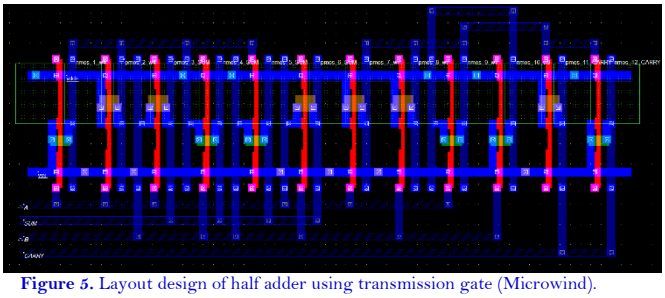

Figure 5. Layout design of half adder using transmission gate (Microwind).

4. RESULTS

The Microwind tool is used in this research study to develop the results. The reason for using these tools is that our objective is to demonstrate the feasibility and proof of concept of the proposed design methodology. However, we can develop the results on more sophisticated industrial tools to further enhance performance. Both the CMOS implementation and the CMOS circuit by the proposed method using a transmission gate are developed in 0.12 µm technology using the Microwind 3.8 tool. The layout's obtained surface area, height, and width are compared. The output results for both the normal and transmission gate approaches and the proposed method are obtained on the Microwind tool and are shown in Figure 6, Figure 7, and Figure 8, respectively.

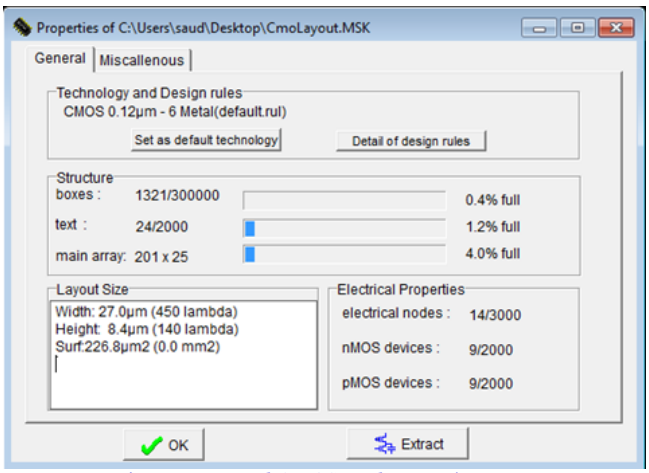

Figure 6. Normal CMOS Implementation.

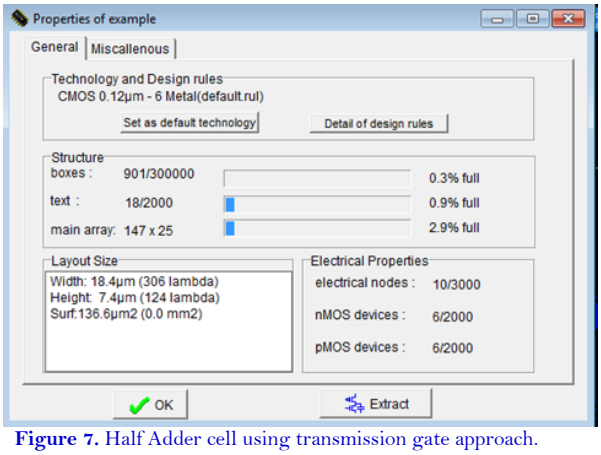

Figure 7. Half Adder cell using transmission gate approach.

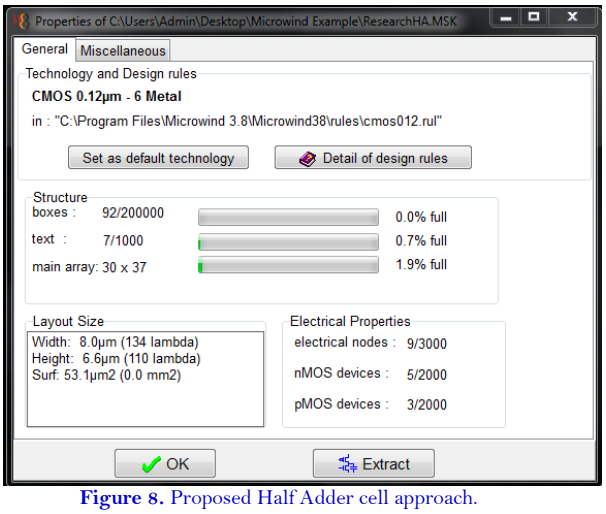

Figure 8. Proposed Half Adder cell approach.

The output functional waveform received on the Microwind tool by considering the input A and B and the outputs SUM and Carry are shown in Figure 9. The stimulus pulses are applied to both the inputs, and the output is recorded. Similarly, we can implement the full adder circuit by using these half adder cells. The full adder cell using two half adders and one OR gate logic implemented. The simulation output of the full adder cell is shown in Figure 10.

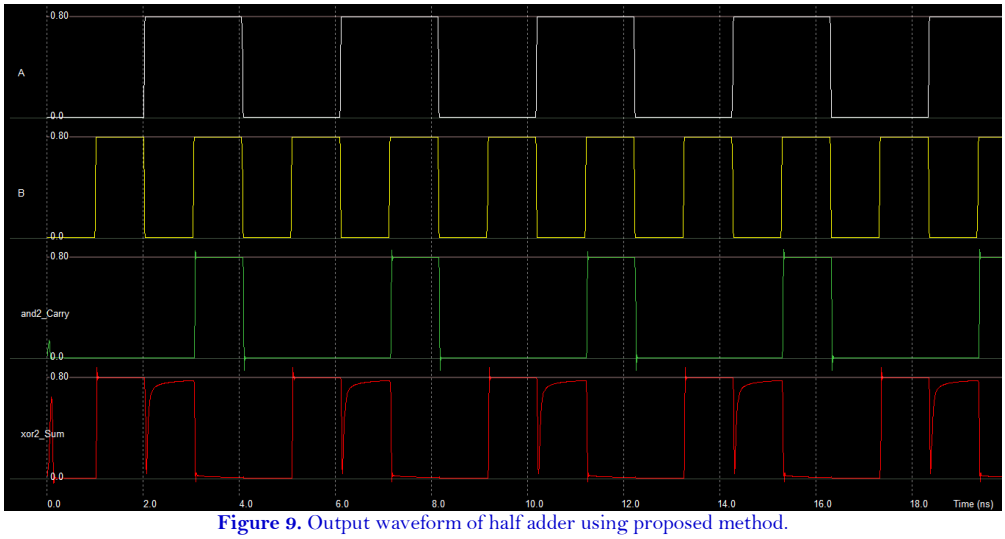

Figure 9. Output waveform of half adder using proposed method.

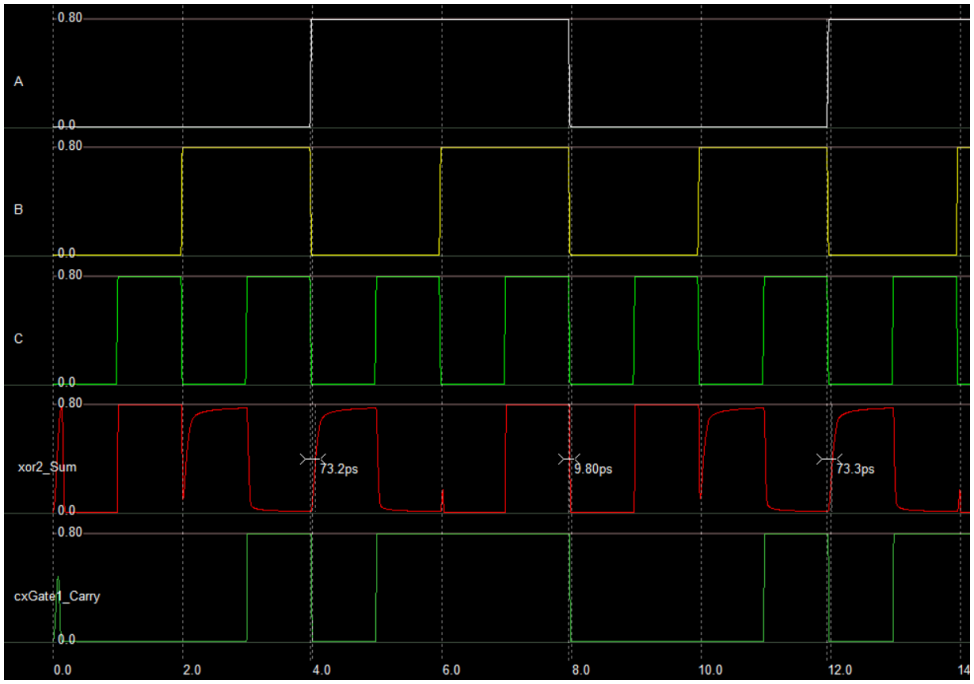

Figure 10. Full adder cell simulation result.

The comparison between the three methods is summarized in Table 1. All three designs are developed on 0.12µm technology, and the Microwind tool has made a comparison of results. It is clearly seen from the results that the proposed method has a significant impact on the area (number of transistors), and thereby on various delays and power consumption when compared with traditional methods.

Table 1. CMOS, Transmission gate, and proposed method results on Microwind tool (CMOS 0.12 µm Technology).

Parameters	CMOS LOGIC	Transmission gate approach	Proposed method
Surface(area)	226.8µm2 (0.0 mm2)	62 µm2 (0.0 mm2)	53.1µm2 (0.0 mm2)
Height of layout	8.4µm2 (140 lambda)	7.4µm2 (124 lambda)	6.6µm (110 lambda)
Width of layout	27.0µm2 (450 lambda)	18.4µm2 (306 lambda)	8.0µm2 (134 lambda)
Power Consumption	90.004µW	35.58µW	3.867µW
Number of Electrical nodes	14	10	9
Number of Transistors	9nMOS + 9pMOS ----➔18	6nMOS + 6pMOS ----➔12	5nMOS + 3pMOS ----➔8

It seems from the results that the total number of transistors used in the case of CMOS logic is 18, and using a transmission gate, 12 transistors. The same logic is implemented by the technique in this research with one transmission gate, two inverters, and one AND gate, using a total of 8 transistors only. The layout design of this proposed method is shown in Figure 11. The power consumption is also reduced significantly, which will have more impact on system design where millions of transistors can be used. The proposed method uses five NMOS and three PMOS transistors to implement the half-adder cell. The length and width of these transistors, and thereby the area of the transistors, are computed and shown in Table II. The proposed transmission gate method has less area and consumes less power than the regular CMOS circuit for small circuits like a half adder. It will have a greater impact when the design becomes more complex. Transistor sizes for the CMOS logic, transmission gate logic, and proposed method cases are compared as the comparison result is tabulated in Table 2.

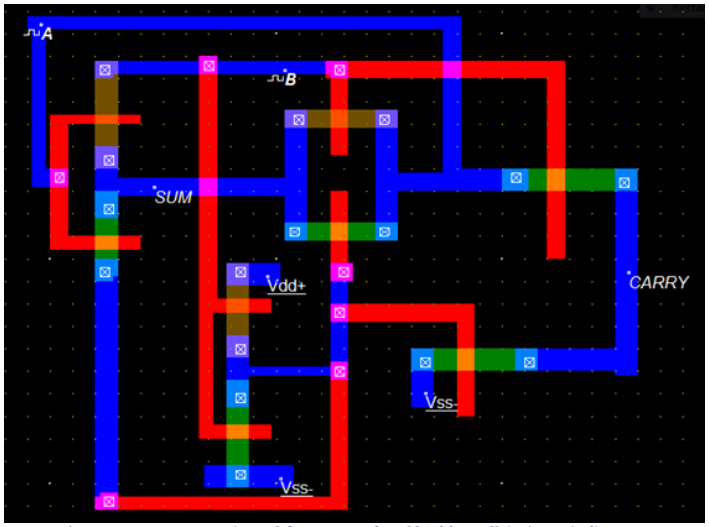

Figure 11. Layout Design of the proposed Half Adder cell (Microwind).

Table 2. Transistor size for the proposed method using transmission gate.

MOS	W (µm)	L (µm)	W (Lambda)	L (Lambda)	Type	Area µm2
N1	0.61	0.12	10	2	Low leakage	0.0792
N2	0.320	0.12	7	2	Low leakage	0.0504
N3	0.20	0.12	4	2	Low leakage	0.0288
N4	0.20	0.12	4	2	Low leakage	0.0288
N5	0.20	0.12	4	2	Low leakage	0.0288
P1	0.710	0.12	11	2	Low leakage	0.0864
P2	0.710	0.12	11	2	Low leakage	0.0864
P3	0.710	0.12	11	2	Low leakage	0.0864

The implementation of the circuits by the various methods in the existing work is compared with the proposed method for area, power, and delay. We implemented the cited works [24-26] using the same tool and similar specifications, allowing us to compare the results. The power, Delay, and area values received on the tool after simulation of the design. The comparison results in terms of the transistor count, power consumption, and delay are shown in Table 3.

Table 3. CMOS vs Transmission gate results on Microwind tool.

Method	Transistor count	Power consumption (µw)	Delay ps	Area µm2
Proposed Method	8	3.867	106	53
Transmission gate	12	35.58	276	62
Transistor Duplication method [24]	18	48.09	456	153
CMOS implementation [25]	18	123	1965	457
CMOS method [26]	18	59.32	693	256

Power consumption and delay are computed, and it helps in finding the Power-Delay Product (PDP). Efficiency and performance are evaluated through the widely used PDP matrix. It is represented as the product of the power consumption (P) and the propagation delay (D) of a circuit. The comparative results on the PDP matrix are given in Table 4.

PDP [femtojoules (fJ)] = P [Power consumption (µw)] * D [Delay (ps)]

Table 4. Power-Delay Product (PDP) matrix for the proposed and other existing methods.

Method	Transistor count	Power consumption (µw)	Delay ps	PDP fJ
Proposed Method	8	3.867	106	0.41
Transmission gate	12	35.58	276	9.82
Transistor Duplication method [24]	18	48.09	456	21.9
CMOS implementation [25]	18	123	1965	242
CMOS method [26]	18	59.32	693	41.1

4.1. Power Reduction Using the Proposed Method

Further, this research has been extended to limit leakage power. We also proposed a novel power reduction technique by limiting leakage in CMOS circuits. The leakage reduction is achieved through a proposed Antileak laydown method with a single bottom sleep PMOS transistor. However, the bottom sleep PMOS can be replaced by an NMOS transistor. This power reduction method can also be applied to FinFET devices. The study's half adder circuit uses one XOR gate, one NAND gate, and one inverter. To understand the concept of leakage reduction, we applied the technique only to the NAND gate cell; however, it can be applied to the entire circuit to reduce leakage and decrease power consumption in CMOS implementation.

The method is applied on the NAND gate as it is considered to perform the experiments. The CMOS NAND gate, a normal CMOS NAND gate is shown in Figure 12 (a), and the proposed Antileak method with a sleep bottom PMOS transistor of the NAND cell, is shown in Figure 12 (b).

We have examined the power consumption of the NAND circuit for the cases of the traditional CMOS method, with the lector method, and with the proposed technique of sleep bottom PMOS. And the obtained output results are tabulated in Table 5.

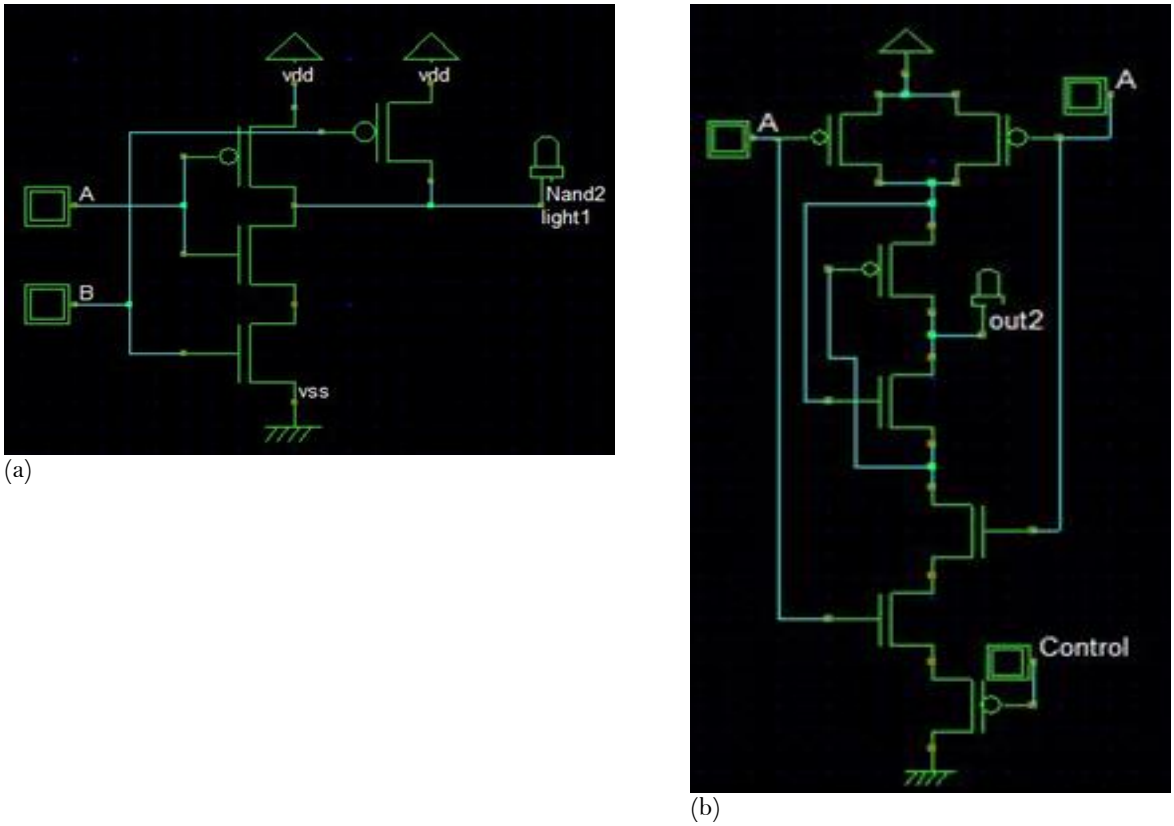

Figure 12. Power reduction circuits for (a) Normal CMOS NAND Gate, (b) CMOS NAND Gate by proposed Antileak PMOS laydown sleep transistor cell.

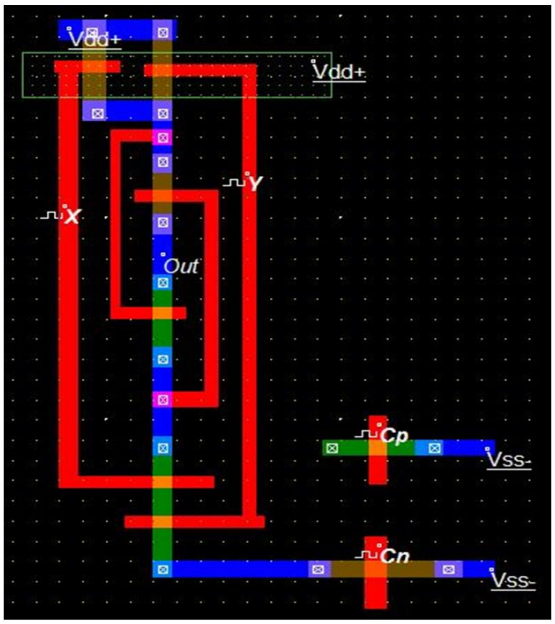

Figure 13. Layout view of the proposed method applied to a NAND gate.

In deep-submicron CMOS technologies, leakage power, especially subthreshold leakage when transistors are "off" becomes a major concern. Proposed antileak and sleep transistors can prevent such issues. In a proposed CMOS NAND circuit, an extra pair of small PMOS and NMOS transistor switches are inserted between the pull-up and pull-down networks. The gates of these inserted transistors are controlled by the internal nodes of the circuit itself, not an external sleep signal, with a very low switching time. This ensures that, in any input combination, at least one of the leakage control transistors is always near its cutoff region, increasing resistance in the leakage path and suppressing leakage even during active mode. However, a PMOS or NMOS transistor at the bottom disconnects the circuit from the supply or ground during idle periods to avoid further leakage problems. When the circuit enters sleep mode, the transistor turns off, cutting the leakage path. Thus, it can suppress leakage at all times, even during active and sleep modes.

We have examined the power consumption of the NAND circuit in the cases of the traditional CMOS method, the lector method, and the proposed technique of sleep- bottom PMOS. The power analysis has been conducted by considering the supply voltage range from 0.1v to 1v in the steps of 0.1v with the fixed output load capacitance, ensuring a typical fan-out condition. The obtained output results are tabulated in Table 5.

Table 5. Result comparison for the NAND gate power consumption for the normal, lector, and proposed Antileak laydown sleep PMOS cell.

NAND gate power consumption n watts			
Supply Voltage	**Normal CMOS**	**LECTOR**	**Proposed**
1	500	320	225
0.9	432	136	87
0.8	394	89.6	27
0.7	313	27.7	4.3
0.6	289	13.8	2.8
0.5	207	3.7	1.7
0.4	167	1.73	0.75
0.3	89	0.96	0.098
0.2	52	0.32	0.002
0.1	0.45	0.09	0.006

The Antileak laydown circuit with bottom sleep NMOS or PMOS layout is obtained by processing different layers on the wafer and is shown in Figure 13. The power consumption is significantly reduced in the proposed

method compared to conventional methods. The comparison graph of the power consumption by the proposed and the other conventional methods is shown in Figure 14.

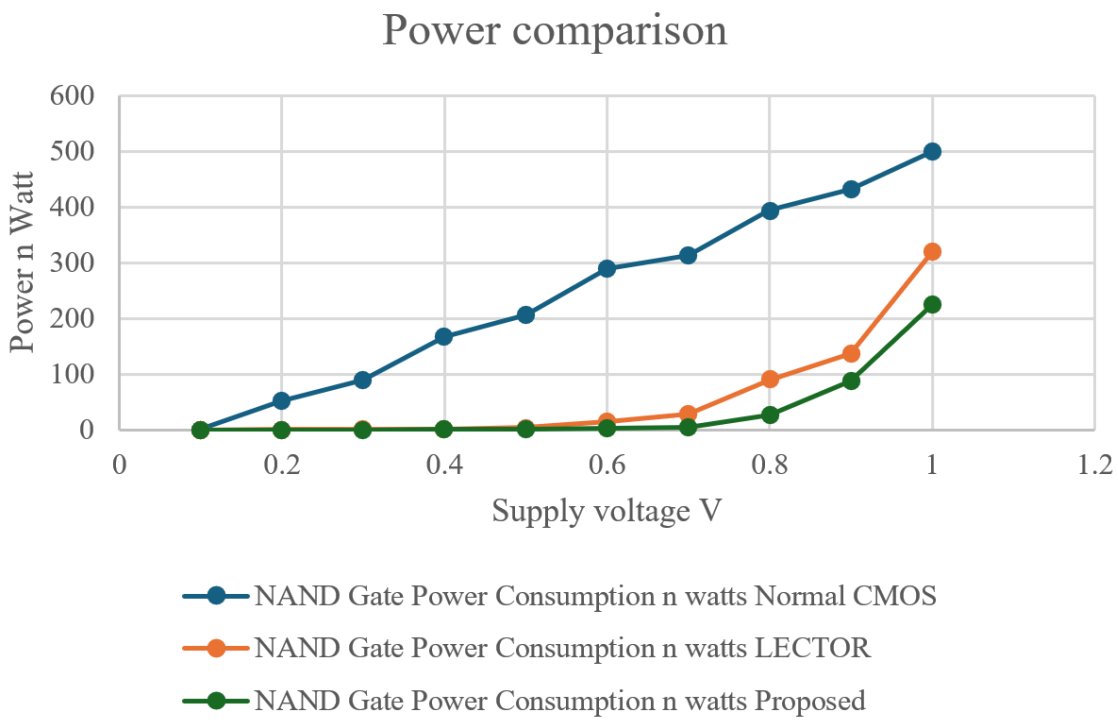

Figure 14. Power consumption graph for the proposed and conventional methods.

5. DISCUSSION

This research proposes a significant method for digital circuit implementation for low-power, low-cost electronic devices to maintain the sustainable semiconductor industry. The CMOS circuit, which was implemented to reduce the transistor count and consequently lower both hardware costs and power consumption, was compared to other conventional methods. The implementation of the CMOS circuit takes the example of a half adder cell, and a NAND gate is included to enhance leakage current performance. The results are compared with the methods [8-11, 24-26] that use CMOS circuits for the hardware count reduction in terms of the transistors used to implement it. Azimi, et al. [24]; El-Maleh, et al. [25] and John [26] proposed the design using 18 transistors to implement the same logic that was implemented in this research study by using only 8 transistors by TG logic. Therefore, this design significantly reduces both area and cost.

The leakage current reduction is also attempted to be reduced by its proposed antileak method using the laydown sleep transistor. The results obtained from the proposed method to reduce the leakage current are compared with those from methods [17-20, 24-26] and the proposed method shows a significantly better performance in terms of leakage current reduction. The paper compares power consumption, delay, and area to conventional methods. The obtained results are significantly better in terms of power consumption. When comparing these results with those from the transistor duplication method and the CMOS implementation method, the advantage is attributed to the proposed antileak method, which limits leakage current and drop in power by 50% by the CMOS method and around 30% by the conventional LECTOR method. By using a small pair of PMOS-NMOS switches that have very low switching times and occupy minimal area, the results obtained by this method in the results section show significant improvements in both area and delay due to the fast switching, self-control gate, and compact size. The comparison results are tabulated, targeting the area, power, and delay. Based on the obtained results, the proposed method plays a significant role in enhancing technology and contributes to maintaining a sustainable semiconductor market.

6. CONCLUSION

This paper presents the method of CMOS circuit design using the transmission gate for a half-adder circuit. This research method reduces the transistor count in the circuits, which in turn decreases the area of the chip while maintaining the circuits' functionality. To address leakage power, the design integrates an Antileak (LECTOR) technique using a pair of self-controlled PMOS–NMOS transistors, which effectively suppress subthreshold leakage without requiring external sleep control signals. Simulation results demonstrate improvements in power consumption and area, with acceptable delay characteristics, when compared with conventional CMOS implementations. The current study is limited to a planar CMOS technology and focuses on a cell-level digital circuit, such as a half-adder. The study did not address advanced technology scaling, interconnect parasitics, or large-scale integration. Future work will extend this design methodology to FinFET-based and sub-7-nm technology nodes and may evaluate its performance when integrated into larger arithmetic units and RISC-V processor blocks, enabling a comprehensive assessment of scalability, power efficiency, and delay at the system level.

Funding: This research was funded by Prince Sattam bin Abdulaziz University, Al-Kharj, Saudi Arabia, through a project grant number (Grant number: PSAU-2024/01/31379).
Institutional Review Board Statement: Not applicable.
Transparency: The authors state that the manuscript is honest, truthful, and transparent, that no key aspects of the investigation have been omitted, and that any differences from the study as planned have been clarified. This study followed all writing ethics.
Competing Interests: The authors declare that they have no competing interests.
Authors' Contributions: All authors contributed equally to the conception and design of the study. All authors have read and agreed to the published version of the manuscript.

REFERENCES

[1] S. Birla, S. Mahanti, and N. Singh, "Leakage reduction technique for nano-scaled devices," *Circuit World*, vol. 47, no. 1, pp. 97-104, 2021. https://doi.org/10.1108/CW-12-2019-0195

[2] M. A. Ahmed and A. M. Abuagoub, "MBIST controller based on March-ee algorithm," *Journal of Circuits, Systems and Computers*, vol. 30, no. 09, p. 2150160, 2021. https://doi.org/10.1142/S0218126621501607

[3] D. M. Badugu, S. S, J. B. Shaik, and R. K. Vobulapuram, "Design of hardened flip-flop using Schmitt trigger-based SEM latch in CNTFET technology," *Circuit World*, vol. 47, no. 1, pp. 51-59, 2021. https://doi.org/10.1108/CW-10-2019-0141

[4] R. Rajaei, M. Tabandeh, and M. Fazeli, "Single event multiple upset (SEMU) tolerant latch designs in presence of process and temperature variations," *Journal of Circuits, Systems and Computers*, vol. 24, no. 01, p. 1550007, 2015. https://doi.org/10.1142/S0218126615500073

[5] D. G. Toro, M. Arzel, F. Seguin, and M. Jézéquel, "Soft error detection and correction technique for radiation hardening based on C-element and BICS," *IEEE Transactions on Circuits and systems II: Express Briefs*, vol. 61, no. 12, pp. 952-956, 2014. https://doi.org/10.1109/TCSII.2014.2356911

[6] S. Lin, Y.-B. Kim, and F. Lombardi, "Design and performance evaluation of radiation hardened latches for nanoscale CMOS," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 19, no. 7, pp. 1315-1319, 2010. https://doi.org/10.1109/TVLSI.2010.2047954

[7] S. Lin, Y.-B. Kim, and F. Lombardi, "Analysis and design of nanoscale CMOS storage elements for single-event hardening with multiple-node upset," *IEEE Transactions on Device and Materials Reliability*, vol. 12, no. 1, pp. 68-77, 2011. https://doi.org/10.1109/TDMR.2011.2167233

[8] V. Ferlet-Cavrois, L. W. Massengill, and P. Gouker, "Single event transients in digital CMOS—A review," *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1767-1790, 2013. https://doi.org/10.1109/TNS.2013.2255624

[9] D. Y.-W. Lin and C. H.-P. Wen, "DAD-FF: Hardening designs by delay-adjustable D-flip-flop for soft-error-rate reduction," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 4, pp. 1030-1042, 2020. https://doi.org/10.1109/TVLSI.2019.2962080

[10] J. Kandpal, A. Tomar, M. Agarwal, and K. K. Sharma, "High-speed hybrid-logic full adder using high-performance 10-T XOR–XNOR cell," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 6, pp. 1413-1422, 2020. https://doi.org/10.1109/TVLSI.2020.2983850

[11] F. Crupi *et al.*, "Understanding the basic advantages of bulk FinFETs for sub-and near-threshold logic circuits from device measurements," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 7, pp. 439-442, 2012. https://doi.org/10.1109/TCSII.2012.2200171

[12] B. P. Shrivastava, S. Sachan, and P. Sachan, "A novel low leakage power reduction CMOS design technique," *Journal of Harbin Engineering University*, vol. 46, no. 5, pp. 1-10, 2025.

[13] V. Dabas and S. K. Grewal, "An optimized 6T XOR circuit using CNTFET technology," *IUP Journal of Telecommunications*, vol. 11, no. 2, pp. 43-56 2019.

[14] S. Garg and T. K. Gupta, "Low power domino logic circuits in deep-submicron technology using CMOS," *Engineering Science and Technology, an International Journal*, vol. 21, no. 4, pp. 625-638, 2018. https://doi.org/10.1016/j.jestch.2018.06.013

[15] T. K. Gupta and K. Khare, "Lector with footed-diode inverter: A technique for leakage reduction in domino circuits," *Circuits, Systems, and Signal Processing*, vol. 32, no. 6, pp. 2707-2722, 2013. https://doi.org/10.1007/s00034-013-9615-2

[16] L. Schmucker, P. Zarkesh-Ha, L. Emmert, W. Rudolph, and V. Gruzdev, "Design of a low-noise subthreshold CMOS inverter-based amplifier with resistive feedback," *Electronics*, vol. 14, no. 5, p. 902, 2025. https://doi.org/10.3390/electronics14050902

[17] N. Onizawa, S. C. Smithson, B. H. Meyer, W. J. Gross, and T. Hanyu, "In-hardware training chip based on CMOS invertible logic for machine learning," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 5, pp. 1541-1550, 2019. https://doi.org/10.1109/TCSI.2019.2960383

[18] N. Oraon and M. Rao, "Stick diagram representation for nanomagnetic logic based combinational circuits," presented at the 2018 IEEE 18th International Conference on Nanotechnology (IEEE-NANO), IEEE, 2018.

[19] P. I. Vaz, P. Girard, A. Virazel, and H. Aziza, "Improving TID radiation robustness of a CMOS OxRAM-based neuron circuit by using enclosed layout transistors," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 29, no. 6, pp. 1122-1131, 2021. https://doi.org/10.1109/TVLSI.2021.3067446

[20] S. I. Huq, S. k. A. Shihab, O. L. Baroi, S. R. Aura, K. M. Ishtiak, and S. N. Biswas, "Low leakage CMOS design technique with stable state retention," *IETE Journal of Research*, vol. 70, no. 4, pp. 4104-4113, 2024. https://doi.org/10.1080/03772063.2023.2208076

[21] Z. Chen, Y. Zhang, Z. Gao, and P. Wan, "Energy-efficient Fe-based FET logic in LUT circuit with transistor reduction technique," *IEICE Electronics Express*, vol. 19, no. 6, p. 20220004, 2022. https://doi.org/10.1587/elex.19.20220004

[22] A. K. Dadoria, K. Khare, T. K. Gupta, and R. Singh, "Ultra-low power FinFET-based domino circuits," *International Journal of Electronics*, vol. 104, no. 6, pp. 952-967, 2017. https://doi.org/10.1080/00207217.2017.1279227

[23] G. Zhou, L. Mao, S. Xie, and C. Min, "A 30Gbps 1.25 pJ/b CMOS receiver analog front-end with low supply voltage," *IEICE Electronics Express*, vol. 18, no. 8, p. 20210114, 2021. https://doi.org/10.1587/elex.18.20210114

[24] S. Azimi, C. De Sio, and L. Sterpone, "A radiation-hardened CMOS full-adder based on layout selective transistor duplication," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 29, no. 8, pp. 1596-1600, 2021. https://doi.org/10.1109/TVLSI.2021.3086897

[25] A. H. El-Maleh, B. M. Al-Hashimi, A. Melouki, and F. Khan, "Defect-tolerant N 2-transistor structure for reliable nanoelectronic designs," *IET Computers & Digital Techniques*, vol. 3, no. 6, pp. 570-580, 2009. https://doi.org/10.1049/iet-cdt.2008.0133

[26] V. John, *Design of a power-efficient Kogge–Stone adder by exploring new OR gate in 45nm CMOS process*. United Kingdom: Circuit World, 2020.

[27] S. S. Sundar and G. Mahendran, "CMOS full adder cells based on modified full swing restored complementary pass transistor logic for energy efficient high speed arithmetic applications," *Integration*, vol. 95, p. 102132, 2024. https://doi.org/10.1016/j.vlsi.2023.102132

[28] M. Hosseinghadiry, H. Mohammadi, and M. Nadisenejani, "Two new low power high performance full adders with minimum gates," *World Academy of Science, Engineering and Technology*, vol. 52, pp. 1077-1084, 2009.

[29] A. Bhargava, G. Salunkhe, A. Yadav, J. J. Gurav, and J. Jeetendra, "Analysis of different CMOS full adder circuits based on different parameters for low voltage," *International Journal of Engineering Research & Technology*, vol. 5, no. 1, pp. 123-130, 2017.