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FPGA IMPLEMENTATION OF MC-CDMA WIRELESS COMMUNICATION SYSTEM BASED ON SDR—A REVIEW

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ABSTRACT

Software Defined Radio (SDR) has the flexibility to modify the characteristics of the receiving and transmitting radio device, without physically adjusting the hardware, due to development in the system. Because of the increasing need for wireless communication applications so as to enable consumers to communicate anywhere through information led to the emergence of many communication devices to include the large amount of applications that every one of the devices needs power and thereby increase the total power. This study confirms that the wireless communication system for secured transmit data, fast and inexpensive; can be done by implementing using Partial Reconfiguration (PR) modern technology in FPGA developing based on SDR. The Speed and performance can be improved. The area also can be decreased. The new Xilinx, Vertex Series FPGA, provides the provision of PR. The power consumption can be reduced by applying power reduction techniques in the blocks. The combination of MATLAB (Simulink and M-file) and Simulink HDL Coder offers flexible capabilities for analysis, design; simulation, implementation, and verification. With all these capabilities, in a single system to reduce the time spent tuning for reducing the algorithms and models during rapid prototyping and experimentation and less time on HDL coding.

Contribution/ Originality: This study contributes in the existing literature review for implementing MC-CDMA wireless communication system using Partial Reconfiguration (PR) that is a new technology in FPGA.

1. INTRODUCTION

The wireless communications revolution started with the mobile phone at the beginning of the 80's and all the improvements which have led to the multiplication of mobile and wireless communications networks and standards [1]. The 1st Generation (1G) of technology was characterized by analog means voice only; 1G quality was too low and also had connections to low speed, but they effectively offered the inherent easiness of mobile communications. The system used in 1G was Frequency Division Multiple Access (FDMA) [2]. The 2nd Generation (2G) of technology is digital in the United States, most of the devices and services were digital. The spread of digital mobile

services is dramatically all over the world. They provide different services such as a certain degree of the facility to access the internet, and digital voice calling and short messaging service. The time division multiple accesses, global system for mobile and code division multiple access used as criteria in 2G. While, generation 3 (3G) of wireless technology has provided faster wireless connections to support more useful services as data, video and multimedia, in addition to audio. The key features of 3G systems are multimedia communications like digital data, audio, video and remote control system, which uses advanced means such as e-mail, fax, paging, cellular phones, surf the Internet, video conferencing, etc., and the ability of high-speed up to more than 2 Mbps and provide the flexibility to direct the repeaters and satellites and local area networks, etc. [3, 4]. The 4th Generation (4G) of wireless technology is still underway. The main difference between 3G and 4G technologies is to increase data transfer rates and security [5]. And 4G looks to provide more improved versions of the same developments that promised to improve the 3G, multimedia and streaming video, global access and worldwide-portability through all types of devices. To some extent, the 4G focuses on video and audio through the use of OFDM technology, and will be able to better allocation of network resources for multiple clients through the use of multiple channels simultaneously. Unlike 3G networks, which combined of package conversion and switched network circuits [3] in systems 4G, it is expected that the data rate target will be up to 1 Gbps for indoor and 100 Mbps of the environments in outdoor. 4G will require the channel capacity of more than 10 times that of 3G systems and must also provide full support for Internet Protocol (IP) [6].

The MC-CDMA technique assigns all users the entire frequency bandwidth at all time and separates users by modulating their signal by unique pseudo noise sequences. This allows the system to be more robust in that the capacity is not fixed, each user is assigned a Pseudorandom Noise (PN) code, this code is overlaid on the information signal, making the signal seem as noise like to all extra users [7]. Combining multi-carrier OFDM transmission with CDMA can benefit from diversity inherent frequency channel broadband through the deployment of each symbol across multiple sub-carriers. This can be the blending of OFDM and CDMA also achieve an average very large user productivity. The benefit of using multiple sub-carriers is that, because every carrier operating on the bit rate is relatively low, and the duration of each symbol a relatively long [8].

Conventional wireless devices no longer meet the needs of the user because it is costly to develop and maintain a wireless system every time a new standard arises into being, where implementation of the MC - CDMA system with the flexibility remains the main problem to bear the practical system. It can achieve the appropriate solution to make communications systems more flexible and easy to use through SDR concept. SDR technology provides multi-band, Multimode, reconfigurability, adaptability, interoperability, and reduces the cost [9]. Through, upgrade of efficiency is providing control software from a variety of modulation/ demodulation techniques. Thus, this technology offers a potentially prolong the life of the product, since the radio can be upgraded efficiency, where efficiency can be measured in terms of cost and physical size consumed per bit of information. Since functions are performed and signal processing for communications systems in SDR, simply by downloading new software, it is possible to deal with different wireless protocols, for the integration of new services and to upgrade to a new standards [10]. Devices such as the DSP and FPGAs are used to implement SDR [11].

There are many algorithms that can be used for the implementation of the SDR in the FPGA. VHDL can be written directly. And also may include a method, Simulink HDL Coder, which makes synthesizable hardware description language code models that have been created to use on a large scale Simulink and State-flow software company automatically. The product produces the goal independent VHDL and Verilog code and test sets for implementation and verification using FPGA. Simulink HDL Coder quickens the design, implementation, and verification of hardware [12] using providing a direct path from system models for programming the FPGA. Simulink HDL Coder creates VHDL and Verilog code, as well as with established hardware implementation and verification apparatuses. As Simulink HDL Coder generates VHDL and Verilog test benches re- use of data that enables simulation systems to verify the implementation of the design [13].

Nowadays, any design in wireless communications is achieved with SDR by Simulink with Matlab and Xilinx design environment. Like the design in an environment with Simulink Xilinx System Generator [14]. DSP structure blocks are provided in Xilinx DSP Block-set library Simulink browser. Make sets of this component of the machine design process easier, more elastic and function simultaneously. Furthermore, modern technology in FPGA called Partial Reconfiguration represents a leap in modern technology. Usually extends partial flexibility inherent in the FPGA by downloading partial bit files, while still remaining logic operates uninterrupted. This is achieved significant benefits most important is to reduce the cost with board space and change the design in the arena and reducing power consuming [15-17].

2. LITERATURE REVIEW

A. Wireless Communication based on SDR and FPGA

Leppanen, et al. [18] introduced a study in software radio as an alternate in the future in wireless own and multimedia communications and discussed its architecture and technical challenges. Also, Murotake, et al. [19] presented the article to review the adaptive processing research and implementation supplies for 2G and 3G base stations considered. Then, the capabilities of certain new monolithic silicon devices are scanned, implementation approach for a reconfigurable multi-mode base station channel modem by SDR design approaches is proposed. It was discussed the improvement of a Hiperlan/I radio modem for the simultaneous transmission of voice, data, and video in the house environment. The modem will finally be integrated with digital set-top box equipment to support wireless internet and digital television applications throughout the house by Sun, et al. [20]. After that, Reves, et al. [21] suggested the feasibility to design and implement a DS-CDMA system based on SDR using FPGA to get fast reconfiguration of the internal system block. Moreover, Kang [22] proposed the design and implementation of the Orthogonal Complex Quadrature Phase Shift Keying (OCQPSK) / Hybrid Binary PSK baseband modem using a DSP chip with consideration of SDR concepts. One modulation scheme is operated by selecting between the two schemes and five physical traffic channels differentiated by orthogonal codes implemented in one DSP chip. In 2002, Tormo and Coquillat [23] introduced (Cardelli et al) optimal implementation of higher performance quadrature direct digital synthesizer technology. The present work every technology mapping phase to amplitude, such as compression techniques ROM and division and coordinate rotation digital computer algorithm, and proposes the structure more appropriate to the segments (FPGA) VIRTEX in order to get the implementation of more efficient in terms of space and productivity. PC-based tool for rapid control and simulation are models for SDR technology. The tool defines a software platform implemented to ease the SDR software style at the analysis, design and implementation steps. SDR is a platform model that provides module and requires the minimal implementation effort to accommodate the device SDR. It has demonstrated the operational use of software models in reducing the difficulty of product design and analysis by Chuang, et al. [24]. In addition, Doan and Le-Ngoc [25] designed an efficient synthesis for interpolation filters for SDR receivers. An adapted farrow structure for the second-order polynomial, symmetric interpreter suitable for low complexity hardware implementation is offered. The complexity, decrease of the modified building has been allowed to fast and simple of implementation. Followed by a year, Blaickner, et al. [26] presented excerpts of the prototyping of runtime reconfigurable processors for application in wireless terminals and base stations and the focus on the multi-standard software defined radio capabilities. Mannan [27] designed and implemented SDR for wireless communication system and compared the different SDR platform. Simulink HDL code was selected for design and implementation. Figure (1) shows the SDR architecture.

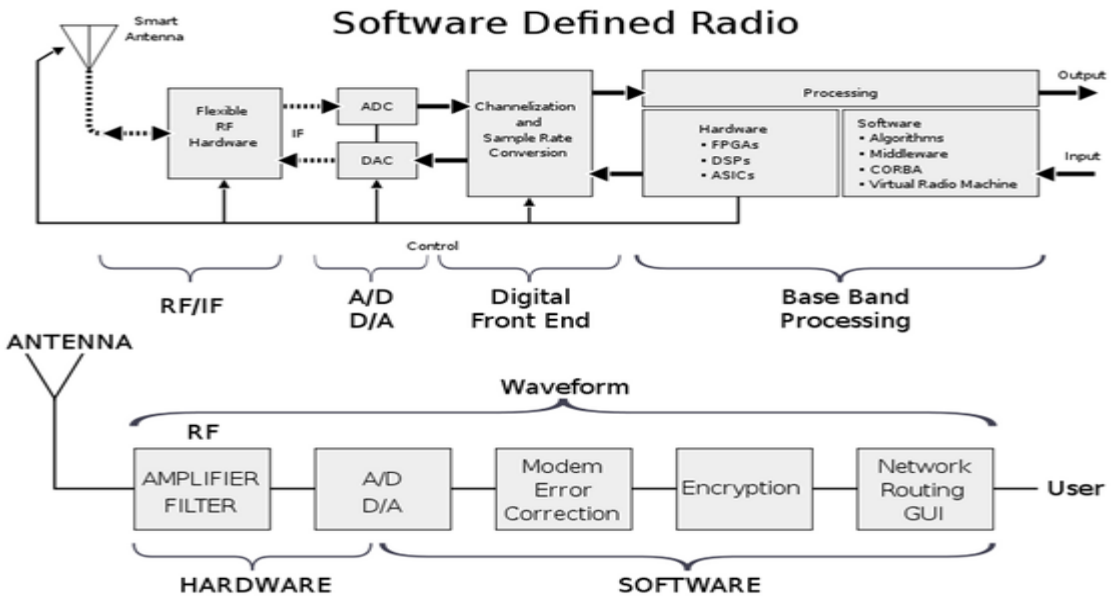

Figure-1. SDR architecture

Source: Blaickner, et al. [26]

Isomaki and Avessta [28] proposed the SDR design flow and platform configuration are modeled as an Integer Linear Programming (ILP) optimization problem. The study of the Bluetooth wireless technology shows, for example. In the same year, Taylor, Green and Taylor [29] described the concept, development, architecture and demo of real-time, software defined four receiver systems and a space-time decoder to be applied on a Xilinx Virtex 2 Pro FPGA. The introduction of the properties of universal radio terminal the techniques are used to obtain multi-mode operation and functionalities of the baseband processing module. They discuss and compare the different approaches for implementing baseband processing unit using reconfigurable architectures by Chaari, et al. [30]. While Garcia, et al. [31] suggested a pipelined CORDIC architecture for designing a scalable and flexible digital cosine and sine wave generator. An FPGA-Based architecture is offered, and the design has been realized on a Xilinx Spartan 3 device. Synthesis and implementation results are shown and discussed. Besides, Vinod, et al. [32] presented a coefficient-partitioning algorithm to achieve high-speed channel filters and low power. Design examples are given of the channel filters employed in the digital advanced mobile phone system and persona unit-standard software defined radio capabilities. Discuss and detail the development of SDR radio portable, powerful and flexible, agile radio called the University Kansas. The principal purpose of KUAR is to enable advanced study in the regions of wireless radio networks, and access to dynamic spectrum and cognitive radios. The KUAR implementation and software, structural are argued carefully. Radio configurations and applications are presented. Display configurations and radio applications. And also search in the future, thanks to the flexibility of this platform by Minden, et al. [33]. Tachwali and Refai [34] were proposed a practical design procedure for the wireless digital modem on SDR platforms and report describe in detail of the baseband signal processing logic design in the FPGA part of it. An outline for designing wireless digital modems on mix software radio stages is discussed.

Elamary, et al. [35] presented a new simple design for a QPSK modulator applied for biomedical device applications. The VHDL programming code is used to generate QPSK digital signals and Altera UP2 development kit board is used for testing the VHDL code modulator. To generate VHDL Code, the direct write of VHDL Code technique is used. While, Jaber, et al. [36] proposed the design procedure and implementation of SDR using Altera Cyclone II family board. MATLAB/Simulink, Embedded Matlab blocks, and Cyclone II development and educational board were used for implementation. Design and progress of a generalized parametrizable modulator can be performed the GMSK modulation and QPSK modulation in a reconfigurable baseband modulator for SDR design. The design has been estimated on FPGA Spartan 3E starter kit by Gurugubelli and Chakrabarti [37]. Moreover, Changrui, et al. [38] provides design and implementation of digital down converter on Xilinx Virtex-5,

over analyzing the key points of the DDC concept and Matlab simulation analysis, DDC with across the clock area and FIFO interface appearances has been designed by Xilinx ISE software. Rodriguez, et al. [39] proposed SDR implementation using Xilinx system generator tools on the Virtex-II FPGA. In the SDR, QPSK is chosen as the modulation scheme for demonstration. A Phase-Locked Loop (PLL) circuit is designed for carrier and symbol synchronization for recovery of data from the received signal. And different encoding scheme is also implemented. It was presented the comparison act in terms of error performance between two modulation techniques, the QPSK, and BPSK. Together modulations were applied on the Spartan 3E starter kit board by Popsscu and Gontena [40].

Furthermore, Tabassam, et al. [41] presented a detailed survey of the existing software and hardware platform for SDR. It also presented a prototype system for testing and designing of SDR in Matlab-Simulink and argues the noticeable functions of the prototype system for CR. Figure (2) depicts the SDR development and roadmap in commercial wireless communication systems. Design the SDR for Spectrum sensing CR that is an innovative technology to increase spectrum usage, by allowing dynamic allocation of the unused spectrum as long as it does not interfere with the main users to whom. It has been licensed by Raut and Kulat [42] found algorithms SDRs for successful data transfer bandwidth available. Through the work of coding modifications, OQPSK to replace QPSK, implementation of Frequency Hopping Spread Spectrum (FHSS) modulation and demodulation in Matlab, to be used to maintain the bits error rate BER at high data rates and modulation techniques for perceptual lossless data compression transmitters and receivers are designed based on the low-power and cost FPGA on the basis of the structure of restructuring can be designed which provides effective communication, So that the design is handled in the simulation environment targeting Xilinx before implementation. As a result gets the design without the complexity and low energy consuming as compared to the conventional systems, and it can also be reconfigured according to the requirement by Bhattacharjee, et al. [43].

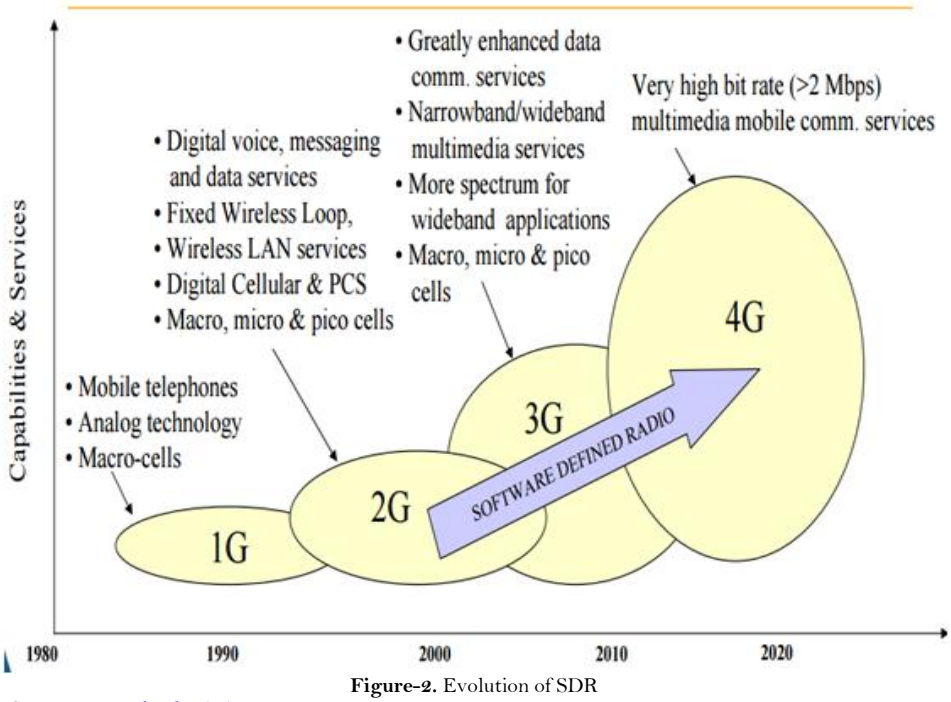

Figure-2. Evolution of SDR

Source: Raut and Kulat [42]

Supriya, et al. [44] presented SDR design by Xilinx System Generator, there is a promising decrease in noise by the design, as shown in Figure (3) transmitter SDR design using Xilinx System Generate.

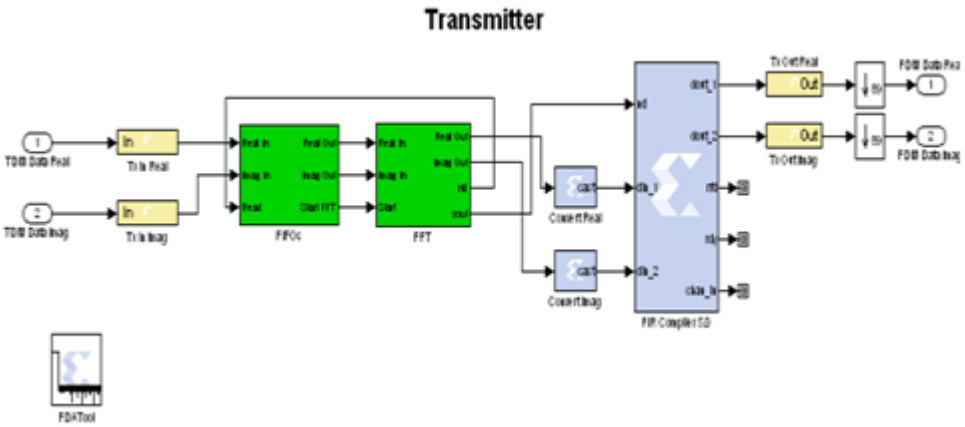

Figure-3. SDR transmitter block

Source: Supriya, et al. [44]

The use of smart antennas, antennas, embedded and reconfigurable antenna group is cheap, depends on the microchip antennas, which will be integrated with the low cost of the GNU Radio SDR test-bed by Donelli and Sacchi [45]. Deployment of OSSIE and its dependencies by submitting porting of OSSIE framework on a custom designed embedded SDR platform, based on Texas Instrument's DAVINCI technology System on Chip (SoC) because Texas instruments integrated provides an efficient platform for applications needing image processing tasks and intensive signal, in addition to general control tasks by Usman, et al. [46]. Perform the design of QPSK modulator for digital signal processing based on DSPs and sliced FPGA that have a certain level of reconfigurability with the use of FPGA integrated circuits, the QPSK modulator could be implemented almost entirely on a single chip along with an indispensable addition of an analog-to-digital converter by Kazaz, et al. [47].

Zhao et al (2013) [48] that they are replaced high- cost USRP by RTL – SDR, with very little cost, which is only used for reception. Where, RTL - SDR has a high-performance DVB-T COFDM (Digital Video Broadcast Terrestrial Coded Orthogonal Frequency Division Multiplexing) demodulator which supports USB 2.0 interface with add mixer RF.

B. The Development of Designs for Wireless Communication System of CDMA with FPGA

Design and implementation of a PN code tracking and data demodulation unit for wideband CDMA PCS system. The PN code is implemented by Altera FPGAs and Tms32oc40 DSPs for flexibility. Timing simulation of the applied system is performed to check the proper operation by Jeong, et al. [49]. Shamain and Milstein [50] provided employ the highest constellation arrangement in conjunction with the CDMA system to develop performance in a multi-user multi-channel and proved to be a severe performance development gained using interference suppression technique above in the case of multi-user continues to hold in a multi-user environment with a narrowband Gaussian intrusion. After that, Jain and Buehrer [51] presented the implementation issues associated with the modulation of adaptive by pilot symbol assisted modulation founded channel estimators for Rayleigh fading environments. Osman [52] describes the DS-CDMA wireless transmitter design using FPGA, four separate blocks have been designed to form the transmitter circuit diagram by the PN-code generator, the oscillator, the BPSK modulator, and the Parity check. The software that has been used for the design, synthesis and simulation is the very high speed integrated circuit hardware description language program that used for coding and FPGA for downloading and compiling the simulation in FPGA. The results of simulated and combined design file by FPGA compiler II were downloaded into the Xilinx Xsv300 FPGA board. DS-CDMA wireless transmitter using FPGA is regarded as a promising technique for future CDMA networks. The transmitter mainly used digital components such as flip-flops, gates, etc., which leads the transmission in higher performance. Design QAM

modulator using multiple four output FIR filters based on Look Up Table was proposed for the downlink of wideband CDMA, and its functions were verified using stand-alone tests by means of the test apparatus that achieved the functions of a QAM receiver system by Park, et al. [53]. Designs and implements a baseband OFDM transmitter and receiver using FPGA. This project focuses on the core processing block of an OFDM system as shown in Figure (4), which are the FFT block and the IFFT. The 8 points IFFT / FFT decimation-in-frequency with radix-2 algorithm analysis in detail to produce a solution that is suitable for FPGA implementation. The FPGA implementation of the project is performed using VHDL. This performance of the coding is analyzed from the result of timing simulation using Altera max plus II [54]. Designs of the direct sequence spread spectrum communication system (DS/SS) using MATLAB-Simulink and then implement it is using Xilinx FPGA devices. First, an MATLAB-Simulink tool is used for designing DS/SS system, and then the logic description of each component in the DS/SS system is derived for the purpose of FPGA application DS/SS system is implemented over Xilinx-Virtex FPGA platform by Al-Shamary [55]. In addition, Carcia and Cumplido [56] presented the design and validation and FPGA-based implementation of an OFDM modulator for IEEE 802.16, by a high-level design device. It was achieved by Xilinx system generator and Simulink of Matlab. The results offered so that it is possible to achieve an OFDM modulator using existing medium density device similar Virtex-II, the results are obtained by Xilinx ISE 6.3I implement.

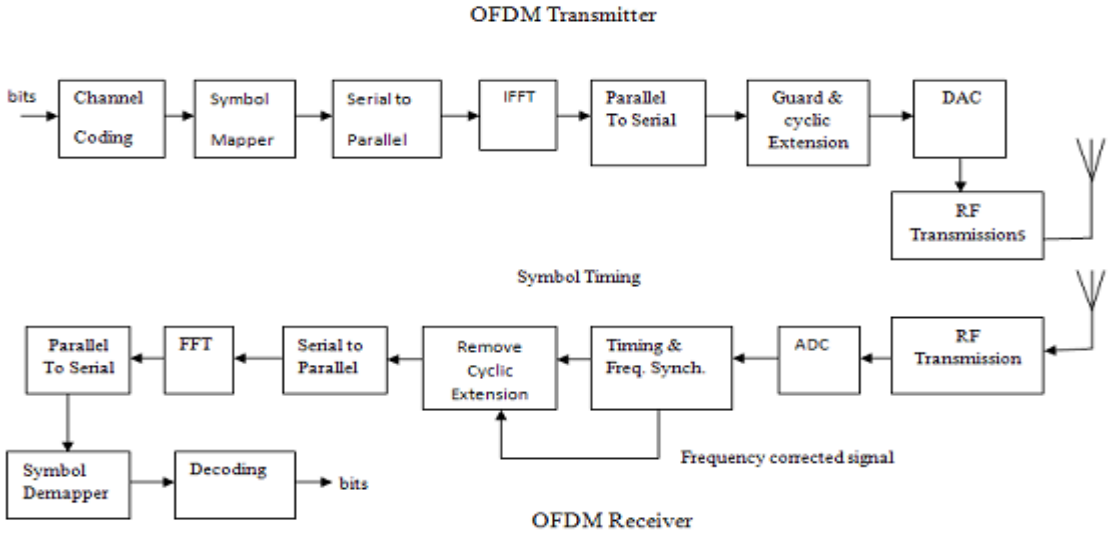

Figure-4. OFDM System Block Diagram

Source: Carcia and Cumplido [56]

Xia and Wang [57] that they discussed the M-QAM modulator for forward link of mulch code-CDMA systems with interference deletion to support high data rate service and provided a logical bit error rate performance of the system. The introduction of analysis of the bit error presentation of the 16-QAM system on Rayleigh fading channels with the highest ratio combining diversity and channel estimate errors by Annarajjala [58]. Furthermore, Kaur [59] discussed the notion of pseudorandom sequences as applicable to spread spectrum communications. Most length sequences were introduced and used as a starter to more complex approaches of PN code generation with the help of Liner Feedback Shift Registers (LFSR). LFSRS modifies itself on every rising edge of the clock. The feedback makes the value in the shift register to cycle through a range of unique values. Explanation of the realization of a Split-Radix FFT processor is based on the structural design of the pipeline. The implementation has been made on FPGA as the medium to get high performance at low prices and a tiny realization time. The CPU has been simulated equal to 350 MHz, through an Ep2s15f672c3 Altera II as a goal device by Carcia, et al. [60]. The design CDMA digital transmitter is an SDR baseband platform. The platform involves of reprogrammable and reconfigurable hardware platform which provides various standards with a shared platform

and focuses also on the approaches of creating VHDL model of CDMA transmitter by Mohamed, et al. [61]. In addition, Alasady and Ibnkahla [62] offered the design technique and implementation results of a 16-QAM lookup table pre-distortion system for satellite communications by Altera DSP board. And, Tuan and Araki [63] proposed the adaptive modulation to increase the throughput of a wireless network using regulating the modulation structure of the channel station. To have more flexibility and more ability by adaptive modulation, the research tries to find a group of modulation systems, which comprises MQAM.

Design and implementation of FPGA transmitter and receiver (Tx/Rx) are used the OFDM. This Tx/Rx OFDM subsystem is capable of dealing with different M-QAM modulations and is implemented in a digital signal processor (DSP-FPGA). The implementation of the Tx/Rx subsystem has been carried out in FPGA using both System Generator visual programming running over Matlab-Simulink, and the Xilinx ISE program which uses VHDL by Gutierrez [64]. The introduction of the easy acquisition system for identifying and finding base stations invisibility in the framework of a CDMA wireless positioning system, based on IS-95 cellular typical by De Angelis, et al. [65]. Concentrating on the importance of MC-CDMA and use adaptive modulation, the exploitation of fluctuations channel quality, so that they can exchange more traffic multimedia is using the same bandwidth, a high efficiency in bandwidth and diversity inherent to the channel fading as compared with OFDM and DS-CDMA in the Figure (5) shown [66].

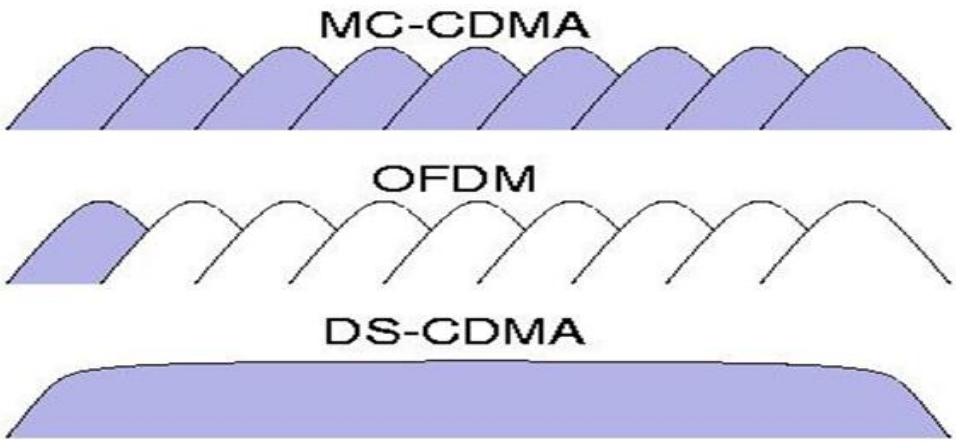

Figure-5. MC-CDMA and DS-CDMA use the whole bandwidth
Source: Nahar and Rahayu [66]

Nahar and Rahayu [67] presented the BER performance of the CDMA cellular scheme based on the IS-95 standard in the existence of an additive white Gaussian noise and interference has been scrutinized. The performance was estimated under two kinds of decision feedback receivers for the CDMA opposite link. Design and implement a baseband OFDM transmitter and receiver on FPGA hardware. All building blocks are designed using VHDL language and then it is implemented using FPGA. On the transmitter part, there are four blocks which consist of the mapper, IFFT, serial to parallel and parallel to serial block. Each of these blocks was tested using FPGA advantages 7.2 software during the design process; the same process was done at the receiver part whereby each of the modules was tested during the design process by Mohamed, et al. [68]. Moreover, Mahbub, et al. [69] proposed an implementation of Direct Sequence-CDMA transmitter by the FPGA. They describe the design for PN coding and a direct sequence principle based wireless transmitter, the circuit for the transmitter is included of basic digital apparatuses, for example, shift registers, flip-flops, PN code and a BPSK modulator. VHDL was used for coding of the design. ModelSim-Altera Edition 6.5b was used for logic verification and functional simulation. The Xilinx Synthesis Technology (XST) v.12.3 was used for the synthesis of the transmitter. Finley, Amsavalli and Kashwan [70] focused on designing and testing the performance of circuits implemented on FPGA for DS-CDMA transceiver using simple circuit concepts, it describes modulation and demodulation circuits for DS-

CDMA. The functional performance of designing circuits is tested by using FPGA and VHDL on XILINX ISE® and MATLAB® platforms. Implementation is carried out on XILINX FPGA chip type xc6vlx75t-3ff484, and simulation is executed using ISE 12.1 version software EDA tool from XILINX. The performance parameter is mainly based on the number of gates used by CDMA sub-circuits and systems in FPGA implementation. Figure (6) illustrations MC-CDMA block diagram.

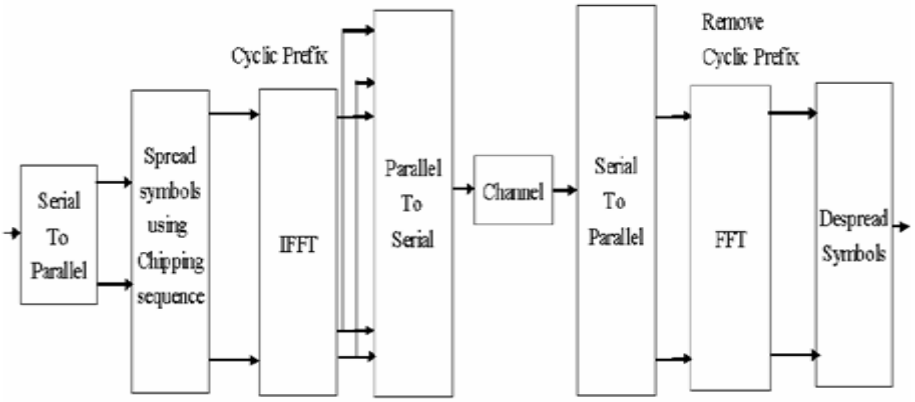

Figure-6. block diagram of the MC-CDMA system [71]

Source: Jaber, et al. [36]

C. Applications of PR in Wireless Communication

Delorme, et al. [72] offered the flow of partial re-configuration to the NOC using a series of telecommunications 4G. Used versions of the tools are available to achieve Xilinx ISE 9.1.2, Plan Ahead 9.2.3, EDK 9.1.2, only two bits-streams have been created for the channel coder PRM because of the restriction on the scheme's performance NOC IP Block. So, performed on the flow of partial reconfiguration of resources with a simple but this methodology not carried out such as FFT, that most complex [72]. Design and implementation of a Partial Reconfiguration (PR) flow method to a series SDR RASIP. This has been made by designing Model handsome 6.0B were conducted for the synthesis of the actual use of the devices on the FPGA, timing analysis and bit stream generation to reshape their Xilinx ISE 9.2i. The design has been implemented on Xilinx Virtex-4 and ML401 board by Kumar, et al. [73]. Figure (7) shows a snapshot Plan Ahead to put the hardware in the FPGA.

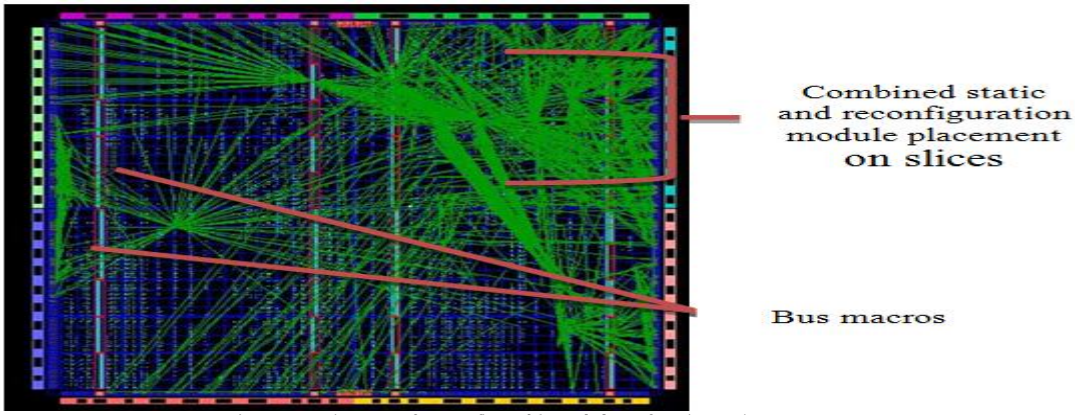

Figure-7. mixtures of Reconfigurable and the reforming unit on FPGA

Source: Kumar, et al. [73]

Ostler, et al. [74] presented an FPGA bootstrapping system for constructing FPGA circuit units using PR [74] where the FPGA at run-time over PCIe, so that this system achieves a slight and static design that is constructed in power even comprises a PCIe endpoint, PR has been used for the caching of hardware, incremental run-time constructing of circuits, and the use of virtual hardware. Evaluation of the application dependent partial

reconfiguration FPGA test process which uses an ASIC BIST method, through Circles Split test and then uses partial reconfiguration to change the role of the division of modules, which may serve as a test or analysis of the response. Sections of the circuit are converted into a format readable (Automatic Test Pattern Generator) ATPG and create test vectors are deterministic. The tool is used to compress the pressure test patterns, as a benefit it is not required to create additional interfaces to access the test or the use of multiple reconfigurations, by Rozkovec, et al. [75]. Design different demodulation technique in Partial Reconfiguration blocks of an FPGA and other signal processing application from an external memory unit can be loaded while the other parts of the FPGA are doing a constant data processing. This SDR design using Xilinx System Generator, terms of used two types of modulation are ASK and PSK by the realization of SDR in PR FPGA to reduce power and increase speed by Joseph and Nirmal [76]. Designing some modules H.264/AVC video encoding on the path reconstruction using DPR, so that this method is not affected productivity and reduce the trade-off is between applications real-time video processing frameworks interfaces. Higher operating frequency is 109.6 MHz and is designed so that easily meets all requirements of the productivity of real-time processing of HTDV, by Orlandic and Svarstad [77]. Hori, et al. [78]; Kumar [79] presented empirically assess the impact of energy and are saving of DPR FPGA *28 nm* process. Using the DPR, it will system require fewer hardware resources, thus, it can provide the energy consumption of the system in The North crypto-processor, is performed only one unit at one-time cipher, and it is overwritten, When it requires a different algorithm. Compared with non-crypto-processor DPR, DPR crypto-processor can cut up to 74% of the mineral resources (slice) and energy consumption 3.4%; Figure (8) illustrates the architecture of DPR.

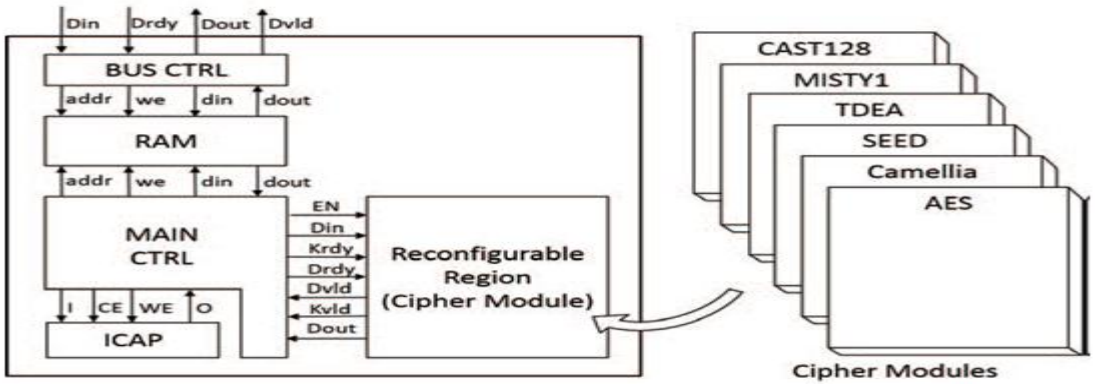

Figure-8. Block diagram of the DPR crypto-processor

Source: Hori, et al. [78]

Kumar [80] used PR in FPGA to design modulation and demodulation so that the user can switch between the modulation schemes and different demodulation through runtime using configuring the control record in FPGA. If the waveform design is made PR then the configuration time and the hardware usage can be kept. Design and implementation of the BPSK, QPSK, 8PSK, and 16PSK modems using PR, So it is the generation of four types of the modulator (M-PSK) By programmable dual-channel terminal-based DDS is given control of the log 2 bits to select the modulation structure and the values of the desired record [81]. In addition, the same design M-PSK, however, it is designed by VHDL code in Modelsim environment to reconfigurable filter and digital NCO so that it can be implemented in Xilinx in addition to Altera FPGAs [80]. Moreover, he presented, Kumar [81] design and Implementation of the 4, 8, 16, 32, 64 -QAM (M-QAM) modulation and demodulation schemes in FPGA using PR, where, the modulator design is composed of a fixed and dynamic part. Module generator phase value, ROM block for storing RRC filter transactions, and the key for IQ mapping constitute a dynamic part. A digital up-converter, it is restructuring RRC filter, control registers 3-bit data type conversion which forms the fixed part. Also, he designed of the OFDM modems using PR faster switch between different OFDM transmitters, that uses 1/2 BPSK, 1/2 QPSK, 3/4QPSK, 1/2 QAM, and 3/4QAM during runtime by configuring the control record in modems FPGA and convolution coding and reed Solomon encoder forming unit coding is given control register 3 bits to

determine a transition plan required and record the values corresponding to each modulation, Figure (9) illustrate fundamental waveform design in FPGA [82]. Furthermore, he Implemented of Digital Pre-Distortion (DPD) using PR with Xilinx soft processor, Microblaze, the implemented DPD is capable of the linear power amplifier used in the system in which it operates multi-transfer schemes, without disturbing the system [83]. Finally, he designed Frequency Hopping Synthesizer (FHS) by using PR; the implemented 256-bit BBS generator is used as the random number generator. The PR approach employed allows the user to change the NCO in minimum time without interrupting the normal working of the system Kumar [84]. Vennila, et al. [85] provided the implementation of the transceiver on the restructuring XILINX VirtexII Pro and be Plan Ahead from XILINX for DPR and undertaken a simulation of a fundamental transmitter and receiver in a cognitive radio system, and the configuration controller is a lookup table based [85].

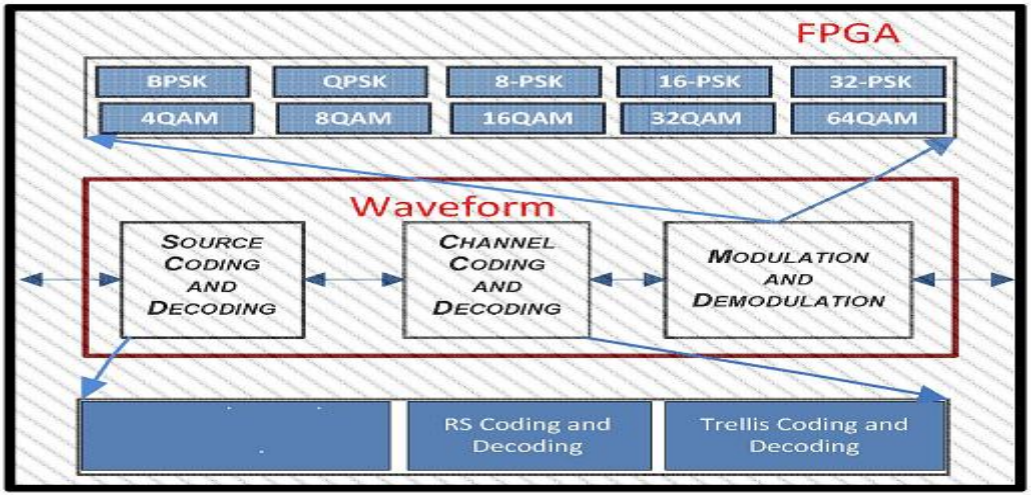

Figure-9. Waveform Design on FPGA

Source: Vennila, et al. [85]

3. DESIGN FLOW FOR WIRELESS COMMUNICATION WITH XILINX SYSTEM GENERATOR

System generator is part of the ISE® Design Suite and provides Xilinx DSP Block-set such as registers, multipliers, adders, filters and memories for application specific design. These blocks take advantage of the generator core XILINX IP to achieve optimal results for the selected device, designs taken with the DSP environment-friendly Simulink modeling using Block-set specific XILINX. It performs all the steps downstream FPGA implementation, including the collection and the place and the way to create a programmable FPGA. The benefit of using the XILINX System Generator for hardware implementation is that the XILINX Block-set provides tight integration with MATLAB, which helps to participate in the simulation unit with FPGA configuration blocks in communications offered by MATLAB blocks [86]. To accomplish the design of the receiver and transmitter devices using Xilinx System Generator needs 2 Software tools to be installed, MATLAB Version R2011a.or higher and Xilinx ISE 13.4. The System Generator token available with Xilinx has to be configured to MATLAB. These results add XILINX block-set for the MATLAB, Simulink environment that can be used directly in the construction of an algorithmic model. The building of wireless circuit components, such as modulation and digital front end, with PR, is using the library provided by Xilinx Block set to support multiple communication standards such as WCDMA, WiMAX, and MC-CDMA. The integration of these components in a single device with FPGA PR and DPR technology to build an SDR system with the architecture less complex and less expensive than through simulation in Matlab Simulink environment and the development of appropriate simulation models and tested. FPGA board can be used here is Spartan6 xc6xls16-3csg324 or Virtex6 or modern. I/O planning and clock planning are implemented model for JTAG hardware co-simulation; the parameters are set generator system

and generated. The assembly is created netlist is to create a project file and a programming model in Verilog HDL, which can be accessed using XILINX ISE. The module checks to examine the behavioral, synthesized and implemented on the FPGA. Xilinx System Generator has generated mainly to deal with complex DSP applications. Bitstream is assembled which is necessary to create an FPGA bit file which is suitable for the input of the FPGA. Figure (10) illustrates the flow of design for XILINX System Generator [87].

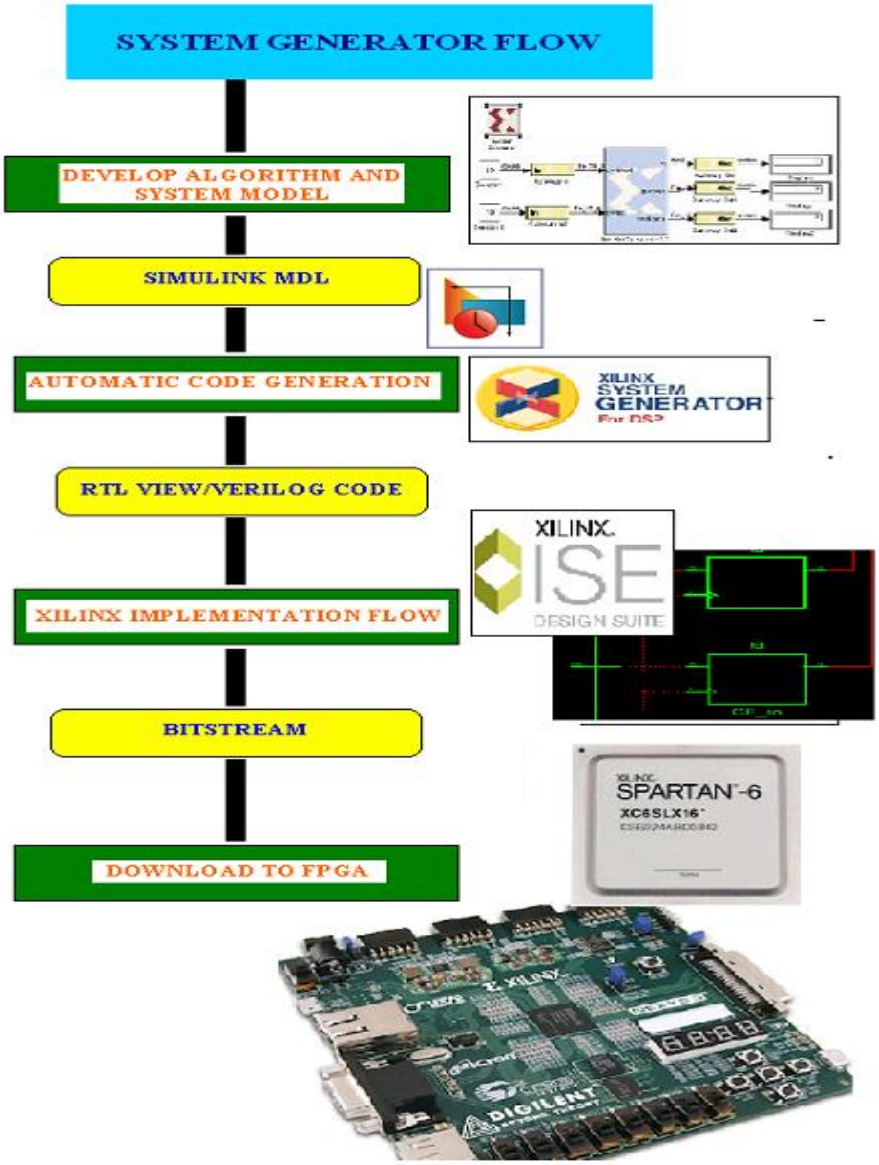

Figure-10. Design flow for Xilinx System Generator
Source: Nahar and Rahayu [67]

3.1. Partial Reconfiguration Design Flow

PR is the capability of reconfigurable hardware to modify logic blocks dynamically without interrupting the system by downloading the smallest bit files. Synthesis flow generates regular BITSTREAM one for programming any FPGA device as an entity that one atomic. In contrast, the flow of PR physically divides the device in the regions, the first is called "static region", which is part of the device that is programmed at startup and never unchangeable, the second is the “dynamic region” and is also known as the "region PR", which is part of the device that will be configured dynamically, potentially several times and with different designs. It is possible to have multiple zones PR. Switching between designs with minimal changes would be faster also bit files corresponding to minor changes will be downloaded to the reconfiguration hardware [88].

Implementing a PR FPGA design is similar to achieve various designs to reshape the non-partial share in a common logic. Designer assigns parts of FPGA to re-composition, on the hand of the physical size of the area and the kinds of resources required. It then describes the designer module different variables that conquer the area, Xilinx FPGAs support re-configuration of block RAM, CLB, and DSP block-sets, addition to all the resources linked with the routing. The ISE software confirms that the resources used to create the tasks of restructuring are enclosed entirely within areas of specific physics, and that any interference occurs with no reconfigure part of the design. Several netlists, represents a static logic and all variable parts of the restructuring of the design, is overloaded into designs and then generates images FPGA design complete with these pieces [88]. Floor-planning, entering constraint, design rule checks are accessed over PlanAhead software. The use of multiple paths through the place and the tools to create Bitstreams path necessary to design all the images partial and full; every pass is a complete design of the FPGA. Once you configure one design to meet all the requests, the designer can re-use the results of the implementation of the establishment of other configurations. After that is the implementation of all configurations, verification procedures to verify uniformity among all versions. Combining all these checks is ensuring a safe environment when loading a partial Bit-stream in the FPGA to run. This is evident in the design flow in Figure (11). After each simulation configuration to make sure that it meets all the requests, designers can generate multiple netlists simulation hierarchy and each validates them on their own or downloaded on the simulator to simulate different combinations of modules that can exist during the operation of the machine [89].

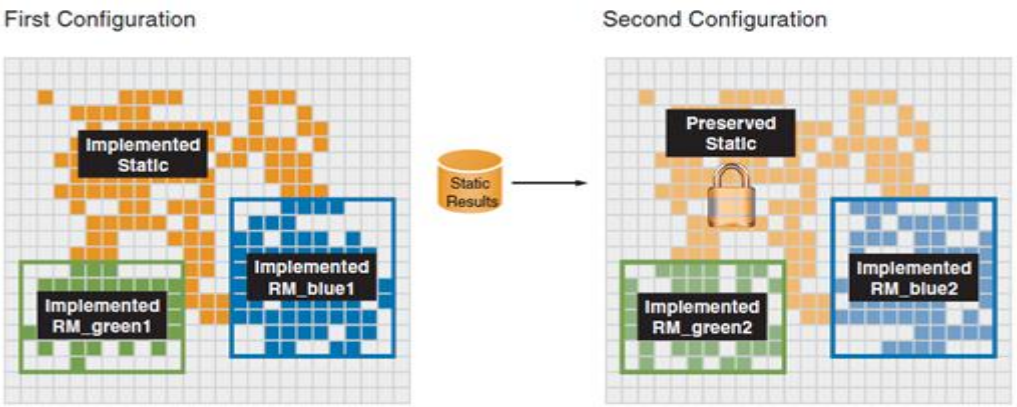

Figure-11. Design Flow of PR

Source: Nahar and Rahayu [89]

Implementation of PR in the field of communications will allow the user to design, build, test, implementation of communication modules in a few minutes instead of a few hours on the FPGA [90].

3.2. The Implementation of MC-CDMA System on FPGA

The Implementation of MC-CDMA System based on FPGA by applying the VHDL code in the Xilinx ISE14.1 program. It is clear; the design can be implemented according to Table 1. In this system with eight bits the transmitter circuit, then tested electronically by using a test bench editor to see its behavior, it gives the desired output on the test bench as shown in Figure (12). In addition, Figure (13) is shown Behavioral Simulation of receiver MC-CDMA System.

Table-1. Final Design Summary of Transmitter for MC-CDMA System

Transmitter Project Status			
Project File:	**Tx_ofdm.xise**	**Parser Errors:**	**No Errors**
Module Name:	Transmitter	Implementation State:	Synthesized
Target Device:	Xc7a100-3csg324	• Errors:	No Errors
Product Version:	ISE 14.1	• Warning:	No Warning
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environments:	System Setting	• Final Timing Scores:	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	17410	126800	13%
Number of Slice LUTs	8044	63400	38%
Number of fully used LUT-FF pairs	8976	96478	9%
Number of bonded IOBs	140	210	66%
Number of Block RAM/FIFO	10	135	7%
Number of BUFG/BUFSCTRLs	2	32	6%
Number of DSP48E1s	176	240	73%

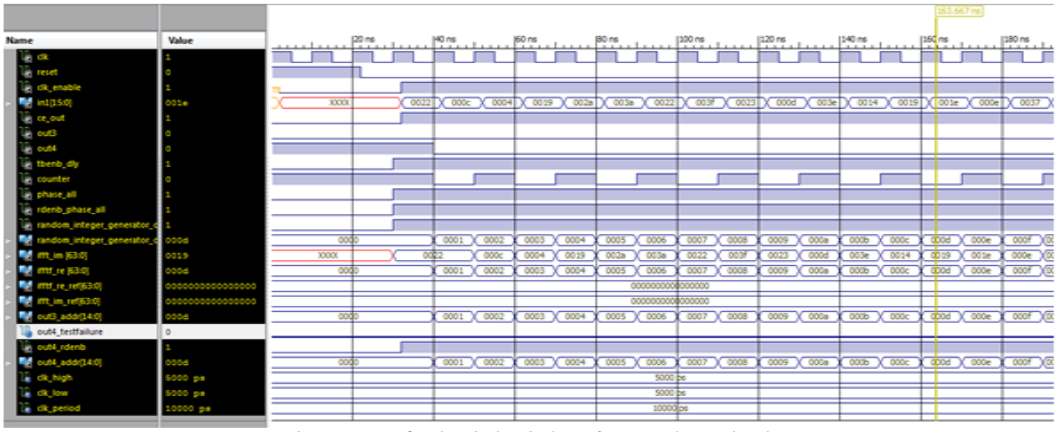

Figure-12. Behavioral Simulation of Transmitter Circuit

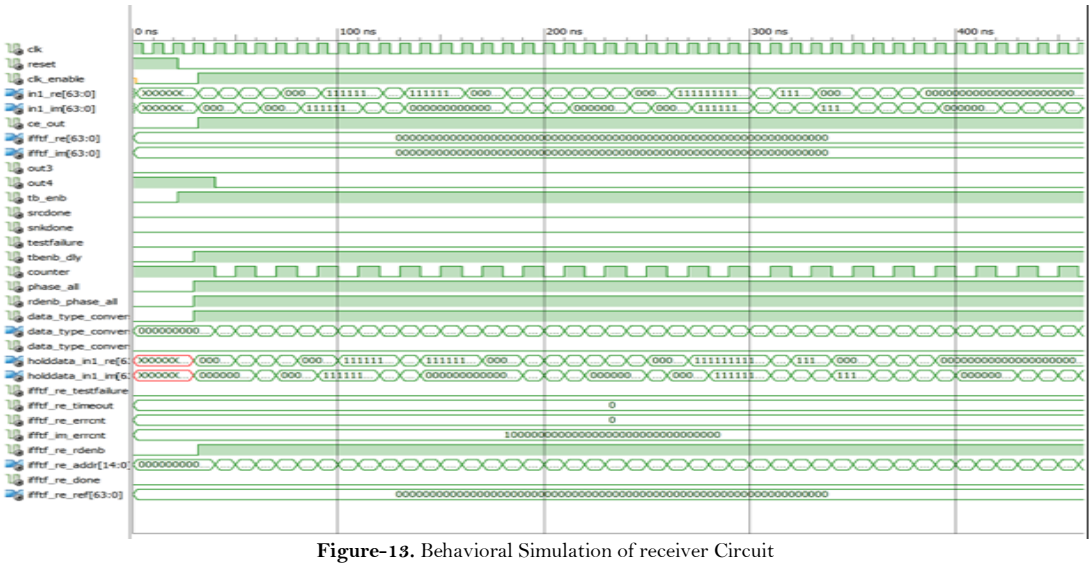

Figure-13. Behavioral Simulation of receiver Circuit

4. CONCLUSION

In this paper, we summarize the review of the wireless communication system based SDR on FPGA. As we address multiple references which were exposed to the evolution of wireless communications using the devices to transmit and receive diverse in the FPGA, and especially those that have been used as a CDMA connection to the many benefits. As we focus on the new technology in FPGA-called partial restructuring and the most important

research with reference to the use of wireless communications is using Xilinx System Generator and Simulink in Matlab. Then we choose MC-CDMA to use with PR in FGPA because, MC-CDMA has solved many problems through the use of cyclic prefix due to higher data rates. It also offers other advantages such as high spectral efficiency, and low complexity implementation and high bandwidth efficiency etc. In addition to this, using of PR is increased the flexibility, reduce the size or number of FPGA, therefore reduce cost, through job sharing time, reduce power consumption, provides real-time flexibility in the choice of algorithms or protocols accessible to the application at any moment, enable the use of PR in the field of security design, Advances FPGA fault tolerance, accelerates configurable computing and reduces storage requirements Bit-stream.

Reconfigurable partial use in transmitters and receivers have become today the work is important for research in recent communications to PR of the benefits of contributing to an increase in the added flexibility and services for users of modern communications technology, which are essential today as the Internet and mobile and data transfer etc. Given that MC-MCDA system high many benefits, and that implementation of this system with distinctive PR, it will produce increase the advantages, and reduce defects and keep pace with rapid growth in demand for wireless communications services.

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